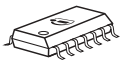
Low Drop Voltage Regulator

TLE 7273

Features

- Output voltage 5 V, 3.3 V or 2.6 V
- Output voltage tolerance ±2% up to I_Q=180mA
- Ultra low quiescent current consumption < 35 µA
- Inhibit function
- Very low dropout voltage
- Reset with adjustable power-on delay
- Window watchdog with current dependent deactivation
- Output protected against short circuit
- Wide operation range: up to 45 V
- Wide temperature range: -40 °C to 150 °C
- Overtemperature Shutdown



P-DSO-14-3, -8, -9, -11, 14

Functional Description

The TLE 7273 is a monolithic integrated voltage regulator with integrated window watchdog and reset dedicated for microcontroller supplies under harsh automotive environment conditions.

Due to its ultra low quiescent current, the TLE 7273 is perfectly suited for applications that are permanently connected to battery. In addition, the regulator can be shut down via the Inhibit input causing the current consumption to drop below 3 µA. The TLE 7273 is equipped with protection functions against overload, short circuit and overtemperature. It operates in the wide junction temperature range from -40 °C to 150 °C.

Derivatives market with "*" have "Target" Status, others have "Final" Status

Type	Ordering Code	Package
TLE 7273 GV50	SP000067155	P-DSO-14-8
* TLE 7273 GV33	Q67006-A9686	P-DSO-14-8
* TLE 7273 GV26	Q67006-A9685	P-DSO-14-8

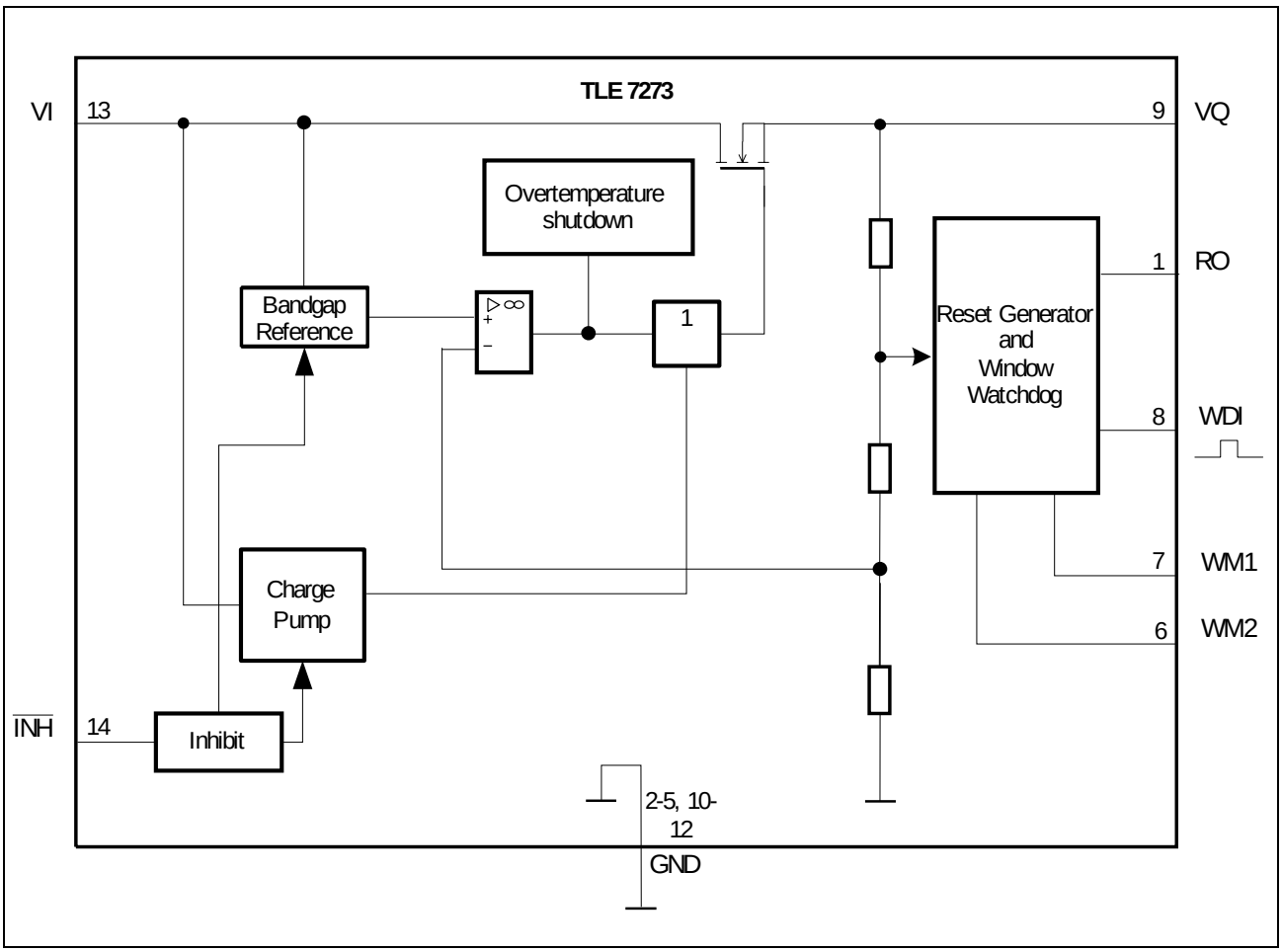


Figure 1 Block Diagram

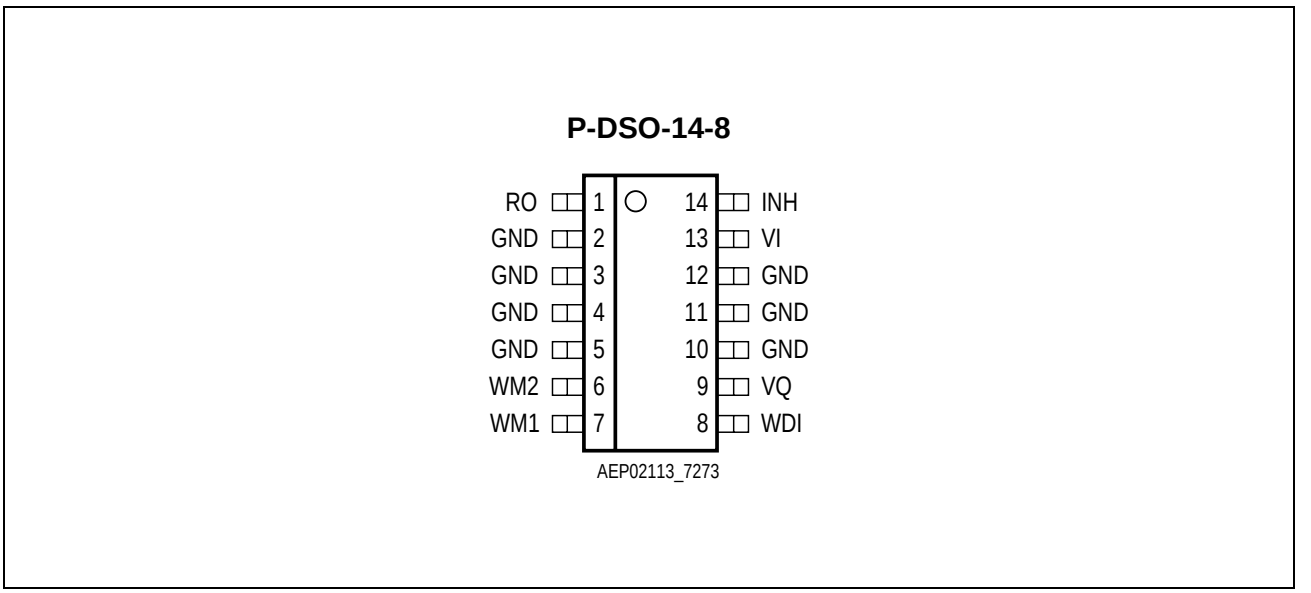


Figure 2 **Pin Configuration** (top view)

Table 1 **Pin Definitions and Functions**

Pin No.	Symbol	Function
1	RO	**Reset Output;** open drain output (TLE 7273 GV33, TLE 7273 GV26). Integrated 20 kΩ pull-up resistor (TLE 7273 GV50). Leave open if not needed.
2-5, 10-12	GND	**Ground;** Pin 2 and 3 must be connected to GND, Pin 4-5, 10-12 should be connected to PCB heat sink area on GND potential.
7	WM1	**Watchdog Mode Bit 1;** Watchdog and Reset mode selection, see **Figure 5**. Connect to V_Q or GND.
6	WM2	**Watchdog Mode Bit 2;** Watchdog and Reset mode selection, see **Figure 5**. Connect to V_Q or GND.
8	WDI	**Watchdog Input;** Trigger Input for Watchdog pulses. Pull down to GND if not needed and turn off the Watchdog with WM1 and WM2 pin.
9	V_Q	**Output voltage;** block to GND with a ceramic capacitor $C_Q \geq 470$ nF close to IC terminal.
13	V_I	**Input voltage;** block to ground directly at the IC with a 100 nF ceramic capacitor
14	$\overline{\text{INH}}$	**Inhibit Input;** low level disables the IC. Integrated pull-down resistor.

Table 2 Absolute Maximum Ratings

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input VI					
Voltage	V_I	-0.3	45	V	–
Current	I_I	–	–	mA	Internally limited
Output VQ					
Voltage	V_Q	-0.3	5.5	V	Permanent
Voltage	V_Q	-0.3	6.2	V	t < 10 s[1)]
Current	I_{Q1}	–	–	mA	Internally limited
Inhibit Input $\overline{\text{INH}}$					
Voltage	$V_{\overline{INH}}$	-1	45	V	–
Current	$I_{\overline{INH}}$	-1	1	mA	–
Reset Output RO					
Voltage	V_{RO}	-0.3	5.5	V	Permanent
Voltage	V_{RO}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{RO}	–	–	mA	Internally limited
Watchdog Input WDI					
Voltage	V_{RO}	-1	7	V	Permanent
Current	I_{RO}	–	–	mA	Internally limited
Watchdog Mode 1					
Voltage	V_{WM1}	-0.3	5.5	V	Permanent
Voltage	V_{WM1}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{WM1}	-5	5	mA	–
Watchdog Mode 2					
Voltage	V_{WM2}	-0.3	5.5	V	Permanent
Voltage	V_{WM2}	-0.3	6.2	V	t < 10 s[1)]
Current	I_{WM2}	–	–	mA	Internally limited

Table 2 Absolute Maximum Ratings (cont'd)

-40 °C < T_j < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
ESD Susceptibility					
Human Body Model (HBM)[2]	Class Voltage	-	2 3	– kV	–
Charged Device Model (CDM)[3]	Class Voltage	-	F6 1.5	– kV	–
Temperatures					
Junction temperature	T_j	-40	150	°C	–
Storage temperature	T_{stg}	-50	150	°C	–

1) Exposure to these absolute maximum ratings for extended periods (t > 10 s) may affect device reliability.

2) ESD HBM Test according JEDEC JESD22-A114

3) ESD CDM Test according JEDEC JESD22_C101

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit. Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as outside normal operating range. Protections functions are not designed for continuous repetitive operation.

Table 3 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Max.		
Input voltage	V_I	5.5	45	V	TLE 7273 GV50
		4.2	45	V	TLE 7273 GV33
		4.2	45	V	TLE 7273 GV26
Junction temperature	T_j	-40	150	°C	–

Thermal Resistances P-DSO-14-8

Parameter	Symbol	Limit Values		Unit	Remarks
		typ..	max.		
Junction pin	$R_{thj\text{-}pin}$	–	25	K/W	Measure to pin 4
Junction ambient	$R_{thj\text{-}a}$	130	–	K/W	PCB, only Footprint[1)]
Junction ambient	$R_{thj\text{-}a}$	90	–	K/W	PCB Heat Sink Area 300 mm^2 [1)]
Junction ambient	$R_{thj\text{-}a}$	80	–	K/W	PCB Heat Sink Area 600 mm^2 [1)]

1) Package mounted on PCB 80 × 80 × 1.5 mm^3; 35µ Cu; 5µ Sn; zero airflow; 85 °C ambient temperature, horicontal PCB-position.

Note: In the operating range the functions given in the circuit description are fulfilled.

Electrical Characteristics

V_I=13.5 V; – 40 °C < T_j< 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output VQ						
Output voltage	V_Q	4.90	5.00	5.10	V	TLE 7273 GV50 1 mA < I_Q < 180 mA 6 V < V_I < 16 V
Output voltage	V_Q	4.90	5.00	5.10	V	TLE 7273 GV50 I_Q = 10 mA 6 V < V_I < 45 V
Output voltage	V_Q	3.234	3.30	3.366	V	TLE 7273 GV33 1 mA < I_Q < 180 mA 4.5 V < V_I < 16 V
Output voltage	V_Q	3.234	3.30	3.366	V	TLE 7273 GV33 I_Q = 10 mA 4.5 V < V_I < 45 V
Output voltage	V_Q	2.548	2.60	2.652	V	TLE 7273 GV26 1 mA < I_Q < 180 mA 4.5 V < V_I < 16 V
Output voltage	V_Q	2.548	2.60	2.652	V	TLE 7273 GV26 I_Q = 10 mA 4.5 V < V_I < 45 V
Output current limitation	I_Q	200	–	500	mA	V_Q = 2.0 V
		200	–	600		V_Q = 0 V
Output drop voltage; $V_{DR} = V_I - V_Q$	V_{DR}	–	250	500	mV	[1] I_Q = 180 mA only TLE7273GV50
Load regulation	$\Delta V_{Q,Lo}$	–	50	90	mV	1 mA < I_Q < 180 mA;
Line regulation	$\Delta V_{Q,Li}$	–	10	50	mV	I_Q = 1 mA; 10 V < V_I < 32 V
Power-Supply-Ripple-Rejection	$PSRR$	–	60	–	dB	f_r = 100 Hz; V_r = 0.5 V_{PP}
Reverse Output Current Protection	V_Q	–	–	5.5	V	I_Q = -1 mA, V_{INH} = 0 V

Electrical Characteristics (cont'd)

V_I=13.5 V; – 40 °C < T_j< 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Consumption						
Quiescent current; $I_q = I_I - I_Q$	I_q	–	–	35	µA	I_Q = 100 µA; T_j<80°C
Quiescent current; inhibited	I_q	–	1	3	µA	V_{INH}= 0V;Tj<80°C
Inhibit Input $\overline{INH}$						
Turn-on Voltage High Signal valid	$V_{\overline{INH}\ ON}$	3.0	–	–	V	V_Q on
Turn-off Voltage Low Signal valid	$V_{\overline{INH}\ OFF}$	–	–	0.4	V	V_Q = 0.02V at I_Q = 5mA
H-input current	$I_{\overline{INH}\ ON}$	–	3	4	µA	$V_{\overline{INH}}$ = 5 V
L-input current	$I_{\overline{INH}\ OFF}$	–	0.5	1	µA	$V_{\overline{INH}}$= 0 V, T_j<80°C
Watchdog Mode Bit 1						
Threshold High Level High Signal valid	$V_{WM1,H}$	4.00	–	–	V	TLE 7273 GV50
		2.65	–	–	V	TLE 7273 GV33
		2.30	–	–	V	TLE 7273 GV26
Threshold Low Level Low Signal valid	$V_{WM1,L}$	–	–	0.80	V	
Watchdog Mode Bit 2						
Threshold High Level High Signal valid	$V_{WM2,H}$	4.00	–	–	V	TLE 7273 GV50
		2.65	–	–	V	TLE 7273 GV33
		2.30	–	–	V	TLE 7273 GV26
Threshold Low Level Low Signal valid	$V_{WM2,L}$	–	–	0.80	V	

Electrical Characteristics (cont'd)

V_I=13.5 V; – 40 °C < T_j< 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog Input WDI						
H-input voltage threshold High Signal valid	V_{WDIH}	4.00	–	–	V	TLE 7273 GV50
		2.65	–	–	V	TLE 7273 GV33
		2.30	–	–	V	TLE 7273 GV26
L-input voltage threshold Low Signal valid	V_{WDIL}	–	–	0.80	V	
H-input current	I_{WDIH}	–	3	4	µA	V_{WDI} = 5 V
L-input current	I_{WDIL}	–	0.5	1	µA	V_{WDI} = 0 V, Tj<80°C
Watchdog sampling time	t_{sam}	0.40	0.50	0.60	ms	Fast watchdog timing
		0.80	1.00	1.20	ms	Slow watchdog timing
Ignore window time	t_{IW}	25.6	32.0	38.4	ms	Fast watchdog timing
		51.2	64.0	76.8	ms	Slow watchdog timing
Open window time	t_{OW}	25.6	32.0	38.4	ms	Fast watchdog timing
		51.2	64.0	76.8	ms	Slow watchdog timing
Closed window time	t_{CW}	25.6	32.0	38.4	ms	Fast watchdog timing
		51.2	64.0	76.8	ms	Slow watchdog timing
Window watchdog trigger time[2)]	t_{WD}	–	48	–	ms	Fast watchdog timing
		–	96	–	ms	Slow watchdog timing
Watchdog deactivation current threshold	I_{Q,WD_off}	0.50	1.50	5	mA	I_Q decreasing V_I > 5.5V for TLE 7273 GV50 V_I > 4.2V for TLE 7273 GV33, TLE 7273 GV26

Electrical Characteristics (cont'd)

V_I=13.5 V; – 40 °C < T_j< 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Watchdog activating current threshold	I_{Q,WD_on}	0.50	1.70	5	mA	I_Q increasing V_I > 5.5V for TLE 7273 GV50 V_I > 4.2V for TLE 7273 GV33, TLE 7273 GV26

Reset Output RO

Output Voltage Reset Switching Threshold	V_{RT}	4.50	4.60	4.70	V	TLE 7273 GV50 V_Q decreasing
		3.00	3.07	3.13	V	TLE 7273 GV33[3)] V_I>4.2V, V_Q decreasing
		2.35	2.38	2.45	V	TLE 7273 GV26[3)] V_I>4.2V, V_Q decreasing
Input Voltage Reset Switching Threshold	V_{RT_VI}	–	3.9	4.0	V	TLE 7273 GV26[3)] TLE 7273 GV33[3)] V_Q>V_{RT}, V_I decreasing
Output Voltage Reset Hysteresis	V_{RH}	–	45	–	mV	TLE 7273 GV26
		–	60	–	mV	TLE 7273 GV33
		–	90	–	mV	TLE 7273 GV50
Reset sink current	I_{RO}	1.75	–	–	mA	TLE 7273 GV50 V_Q=4.5V,V_{RO}=0.25V
		1.30	–	–	mA	TLE 7273 GV33 V_Q=3.0V,V_{RO}=0.25V
		1.10	–	–	mA	TLE 7273 GV26 V_Q=2.35V,V_{RO}=0.25V
Reset output low voltage	V_{ROL}	–	0.15	0.25	V	$V_Q \geq$ 1 V; I_{RO} < 200 µA
Reset high voltage	V_{ROH}	4.5	–	–	V	TLE 7273 GV50
Reset high leakage current	I_{ROLK}	–	–	1	µA	TLE 7273 GV33 TLE 7273 GV26

Electrical Characteristics (cont'd)

V_I=13.5 V; – 40 °C < T_j< 150 °C; unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Integrated reset pull up resistor	R_{RO}	10	20	40	kΩ	TLE 7273 GV50 Internally connected to V_Q
Power-on Reset delay time	T_{RD}	12.8	16.0	19.2	ms	Fast reset timing
		25.6	32.0	38.4	ms	Slow reset timing
Reset Reaction Time	T_{RR}	-	4	12	µs	

1) measured when the output voltage has dropped 100 mV from the nominal Value obtained at V_I=13.5V.
2) Recommendation for typical trigger time. $t_{WD}=t_{CW}+1/2*t_{OW}$
3) Reset Output triggered when Output Voltage V_Q is lower than Output Voltage Reset Switching Threshold V_{RT} or is also triggered, when Input Voltage is decreasing to V_I<4.0V and VQ>V_{RT}

Circuit Description

Power On Reset and Reset Output

For an output voltage level of $V_Q \geq 1$ V, the reset output is held low. When the level of V_Q reaches the reset threshold V_{RT}, the signal at RO remains low for the power-up reset delay time T_{RD}. The reset function and timing is illustrated in **Figure 3**. The reset reaction time T_{RR} avoids wrong triggering caused by short “glitches” on the V_Q-line. In case of V_Q power down ($V_Q < V_{RT}$ for $t > T_{RR}$) a logic low signal is generated at the pin RO to reset an external microcontroller.

The TLE 7273 GV50 features an integrated pull-up resistor on the reset output while the TLE 7273 GV33 and TLE 7273 GV26 have an open drain output requiring an external pull-up resistor ≥ 5.6 kΩ[1]. At low output voltage levels $V_Q < 1$ V the integrated pull-up resistor of the TLE 7273 GV50 is switched off setting the reset output high ohmic. Example: Calculation based on the reset sink current and an external pull-up resistor connection to 5V:

$R_{extmin} = dU / I_{RO} = (V_{RTmin} - V_{ROmin}) / I_{RO} = (4.5V - 0.25V) / 1.75mA = 2.42kOhm$

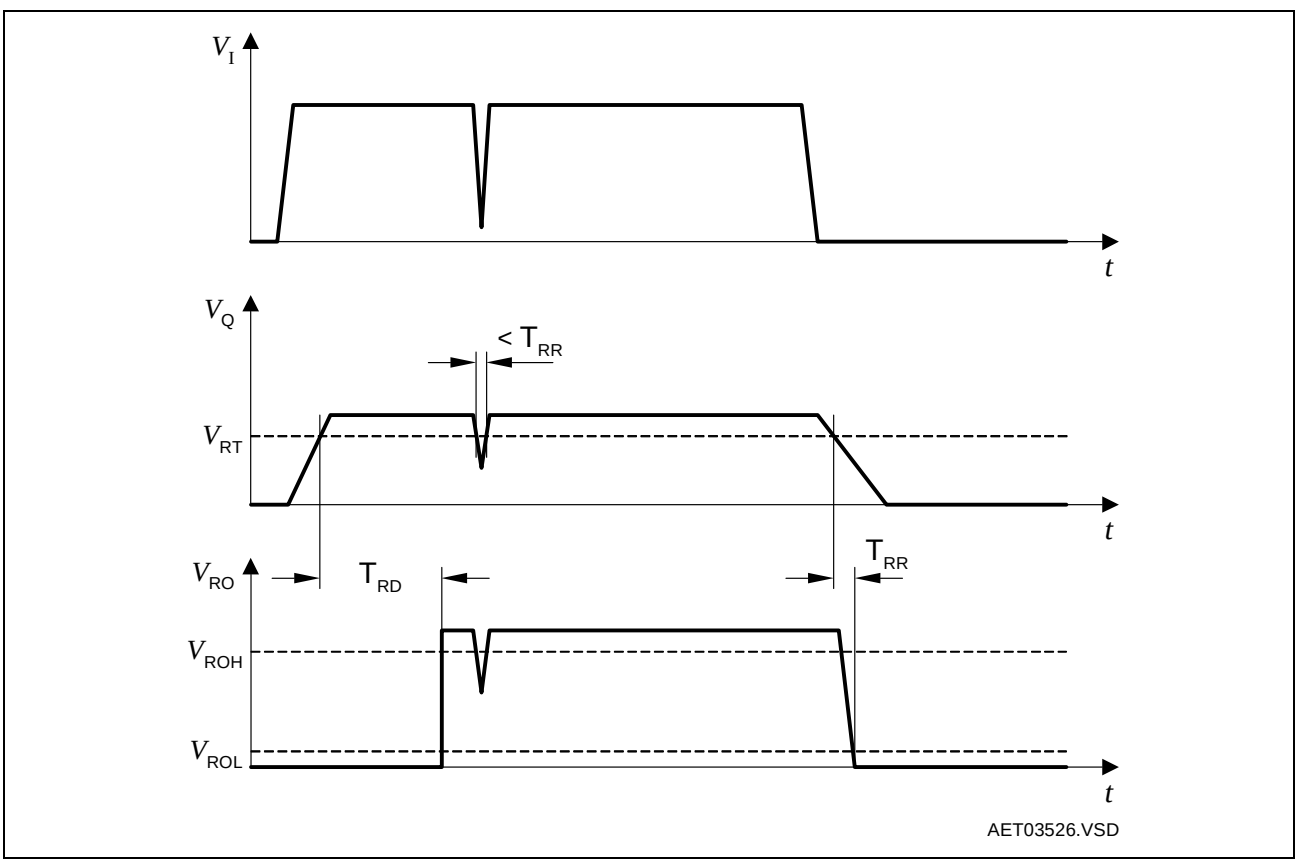


Figure 3 Reset Function and Timing Diagram

1) Referred to pull-up voltage level of 5 V.

Application Circiut

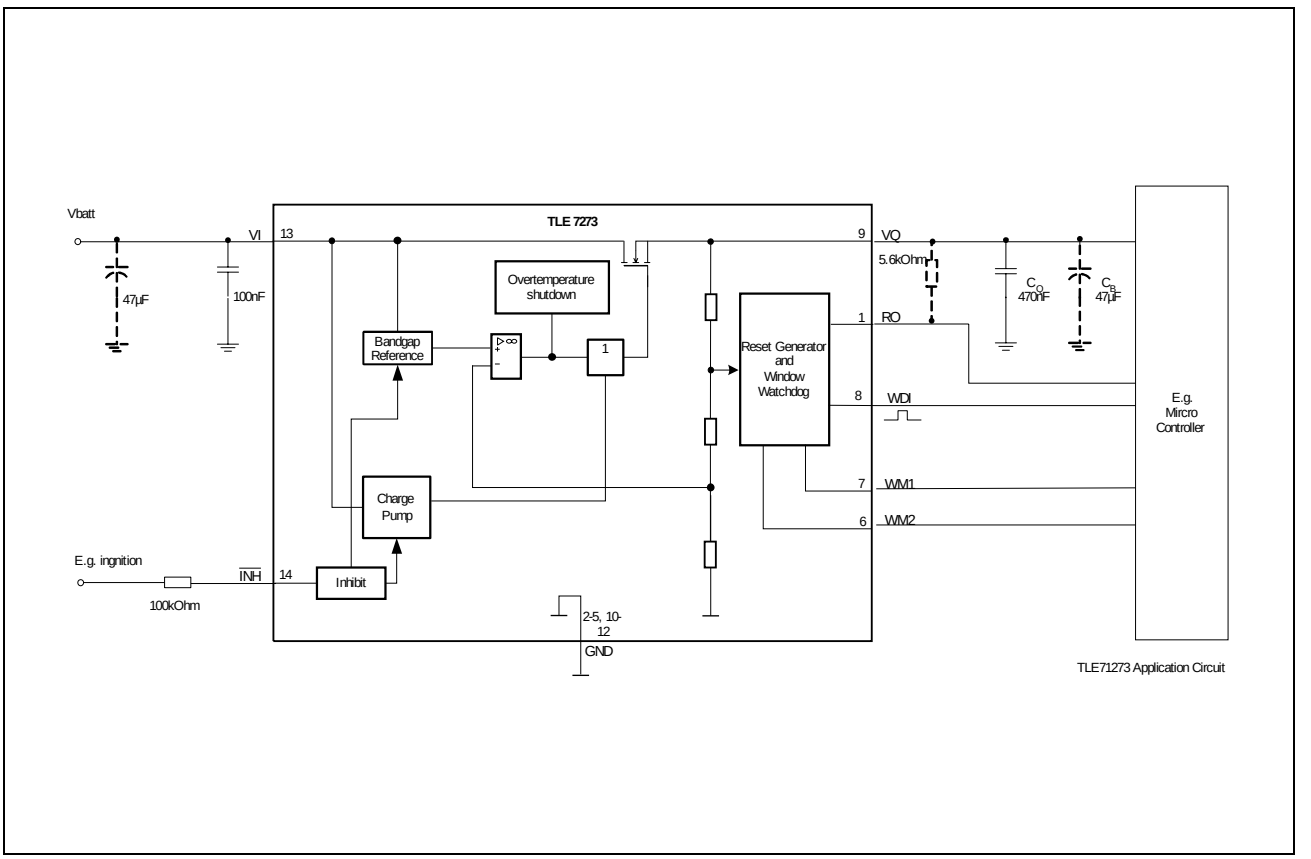


Figure 4 Application Diagram

A typical application of the TLE 7273 is shown in Fig.4. To prevent the regulation loop from oscillating a ceramic capacitor ≥ 470nF is required at the output V_Q. In contrast to most low drop voltage regulators, the TLE 7273 only needs moderate capacitance at the output and tolerates ceramic capacitors to keep the stability. This offers more design flexibility to the circuit designer enabling also to operate the device without tantalum capacitors.

Additionally, a blocking capacitor C_B of 10 … 47 µF should be used for the output VQ to suppress influences from load surges to the voltage levels. This one can either be an aluminum electrolytic capacitor or a tantalum capacitor following the application requirements.

A general recommendation at Tj<90°C is to keep the drop over the equivalent serial resistor (ESR) of the blocking capacitor C_B together with the discharge of the blocking capacitor below 300mV. Since the regulator output current roughly rises linearly with time the discharge of the capacitor can be calculated as:

$$dVC_B = dI_Q * dt / C_B$$

The drop across the ESR calculates as:

$$dV_{ESR} = dI*ESR$$

To prevent a reset the following relationship must be fullfilled:

$$dV_C + dV_{ESR} < 300mV$$

Example: Assuming a load current step of dI_Q = 50mA, a blocking capacitor of C_Q = 22µF and a typical regulator reaction time under normal operating conditions of dt ~ 25µs and for special dynamic load conditions, such as load step from very low base load, a reaction time of dt ~ 75µs.
For this expample the typical condition is considered and the calculation is done based on dt = 25µs:

$$dV_C = 0.1A * 25µs/22µF = 114mV$$

So for the ESR we can allow

$$dV_{ESR} = 300mV - 114mV = 186mV$$

The permissible ESR becomes:

$$ESR = 186mV/100mA = 1.86Ohm$$

During design-in of the TLE7273 product family, special care needs to be taken with regards to the regulators reaction time on sudden load current changes starting from very low pre-load as well as cyclic load changes. The application note "*TLE7x Voltage Regulators - Application Note about Transient Response at ultra low quiescent current Voltage Regulators*" (see 3_cip05405.pdf) gives important hints for successful design-in of the Voltage Regulators of the TLE7x family.

Watchdog Operation

The watchdog uses a fraction of the charge pump oscillator's clock signal as timebase. The watchdog timebase can be adjusted using the pins WM1 and WM2 (see **Figure 5**). The watchdog can be turned off setting WM1 and WM2 to high level. The timing values refer to typ. values with WM1 and WM2 connected to GND (fast watchdog and reset timing).

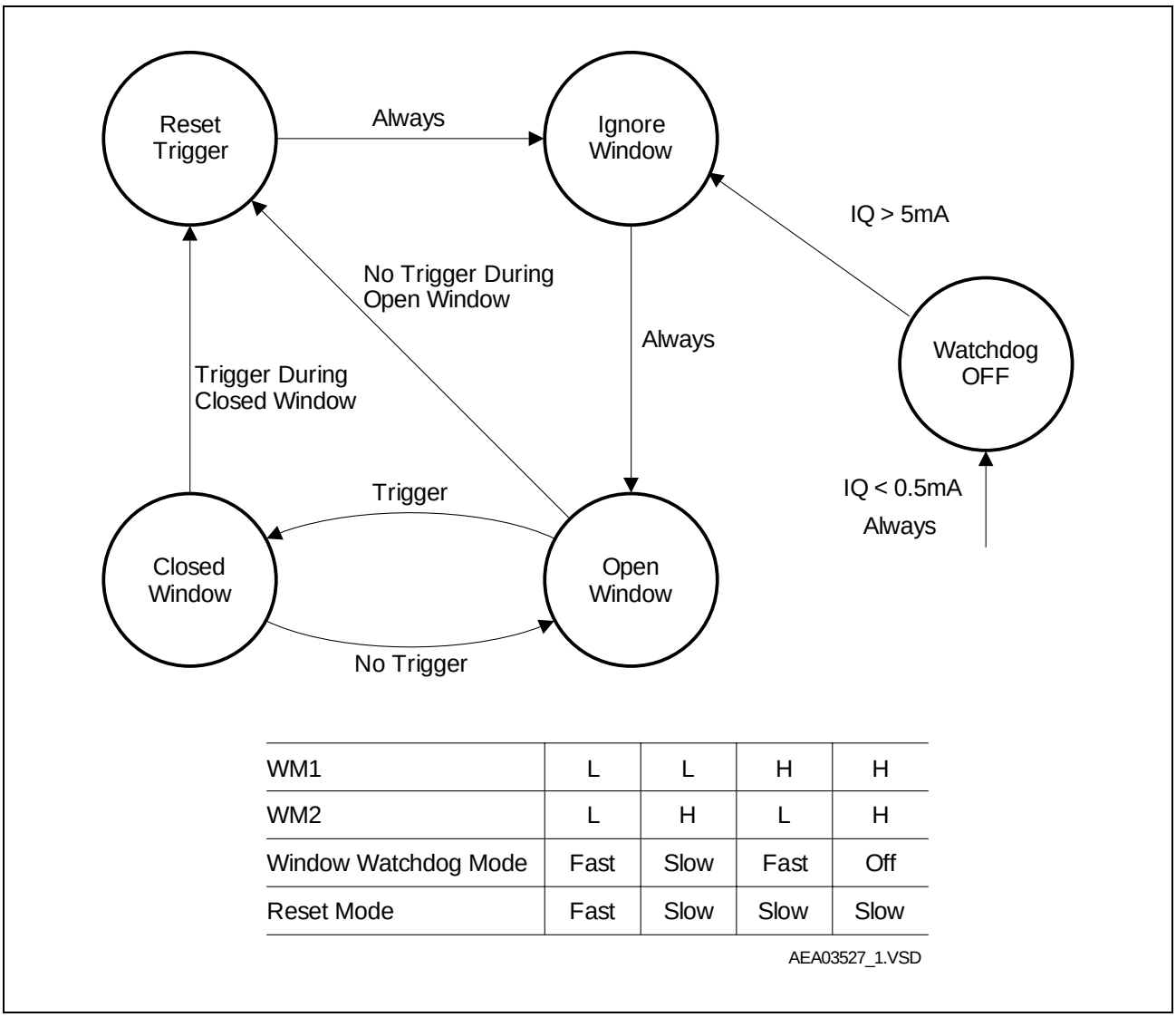
Figure 5 shows the state diagram of the window watchdog (WWD) and the watchdog and reset mode selection. After power-on, the reset output signal at the RO pin (microcontroller reset) is kept LOW for the reset delay time T_{RD} of typ. 16 ms. With the LOW to HIGH transition of the signal at RO the device starts the ignore window time t_{CW} (32 ms). During this window the signal at the WDI pin is ignored. Next the WWD starts the open window which is in the very first turn after power up a long open window with tmax = 4 * t_{OW}. In the following turns, the timing corresponds to the standard timing setting as described in the specification.

When a valid trigger signal is detected during the open window a closed window is initialized immediately. A trigger signal within the closed window is interpreted as a pretrigger failure and results in a reset. After the closed window the open window with the duration t_{OW} is started again. The open window lasts at minimum until the trigger process has occurred, at maximum t_{OW} is 32 ms (typ. value with fast timing).
A HIGH to LOW transition of the watchdog trigger signal at pin WDI is considerede as a valid trigger pulse.

See **Figure 7**: To avoid wrong triggering due to parasitic glitches two HIGH samples followed by two LOW samples (sample period t_{sam} typ. 0.5 ms) are decoded as a valid trigger .

A reset is generated (RO goes LOW) if there is no trigger pulse during the open window or if a pretrigger occurs during the closed window. The triggering is correct also, if the first three samples (two HIGH one LOW) of the trigger pulse at pin WDI are inside the closed window and only the fourth sample (the second LOW sample) is taken in the open window.

After turning OFF the Watchdog by output current reduction, RO remains high. (see also the signal diagram in **Figure 6**). After turning ON the WWD again by exceeding the current threshold, the logic cycle starts again with the Ignore Window and goes then into the "1st. long open window". This 1st long OW is maximum 4 * t_{OW} long and allows the re-synchronisation between the micro controller and the WWD timing. The 1st. long OW is closed by the first valid trigger on WDI from the mirco controller. This trigger ensures the synchronisation. As soon as this trigger is done, the micro controller timing must be stable and correspondent to t_{WD} .



WM1	L	L	H	H
WM2	L	H	L	H
Window Watchdog Mode	Fast	Slow	Fast	Off
Reset Mode	Fast	Slow	Slow	Slow

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Figure 5 Window Watchdog State Diagram, Watchdog and Reset Modes

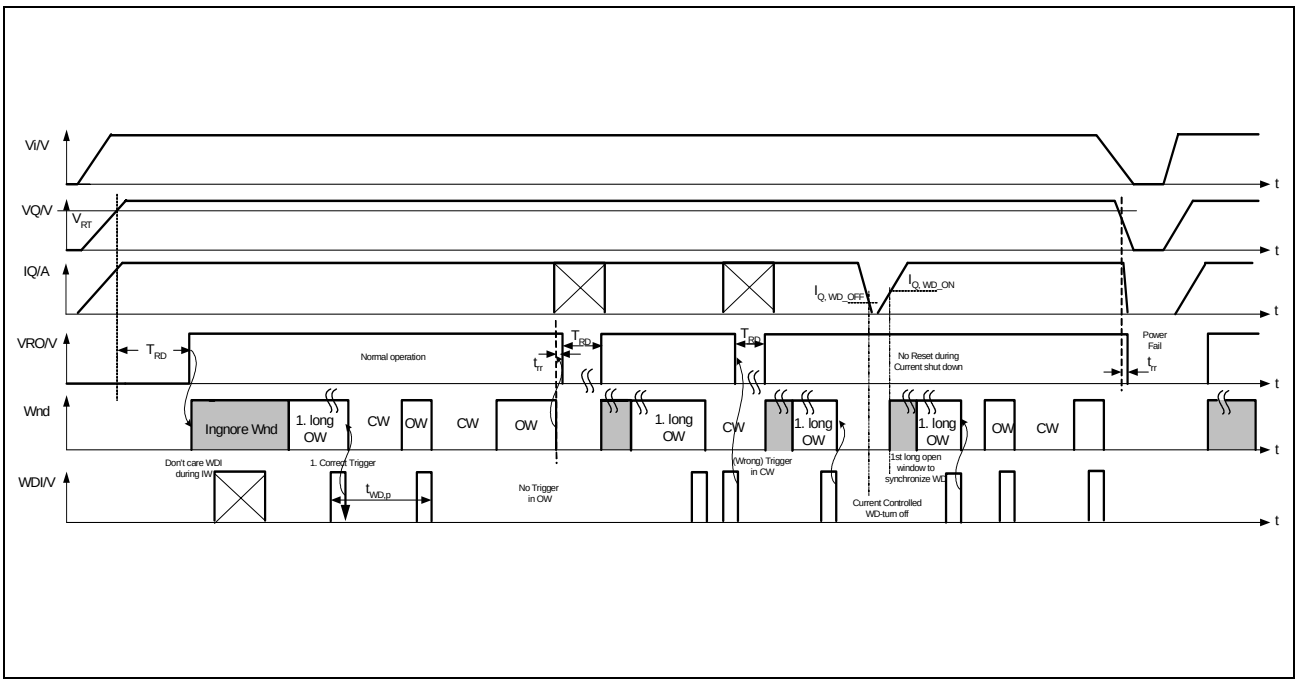


Figure 6 Window Watchdog Signal Diagram

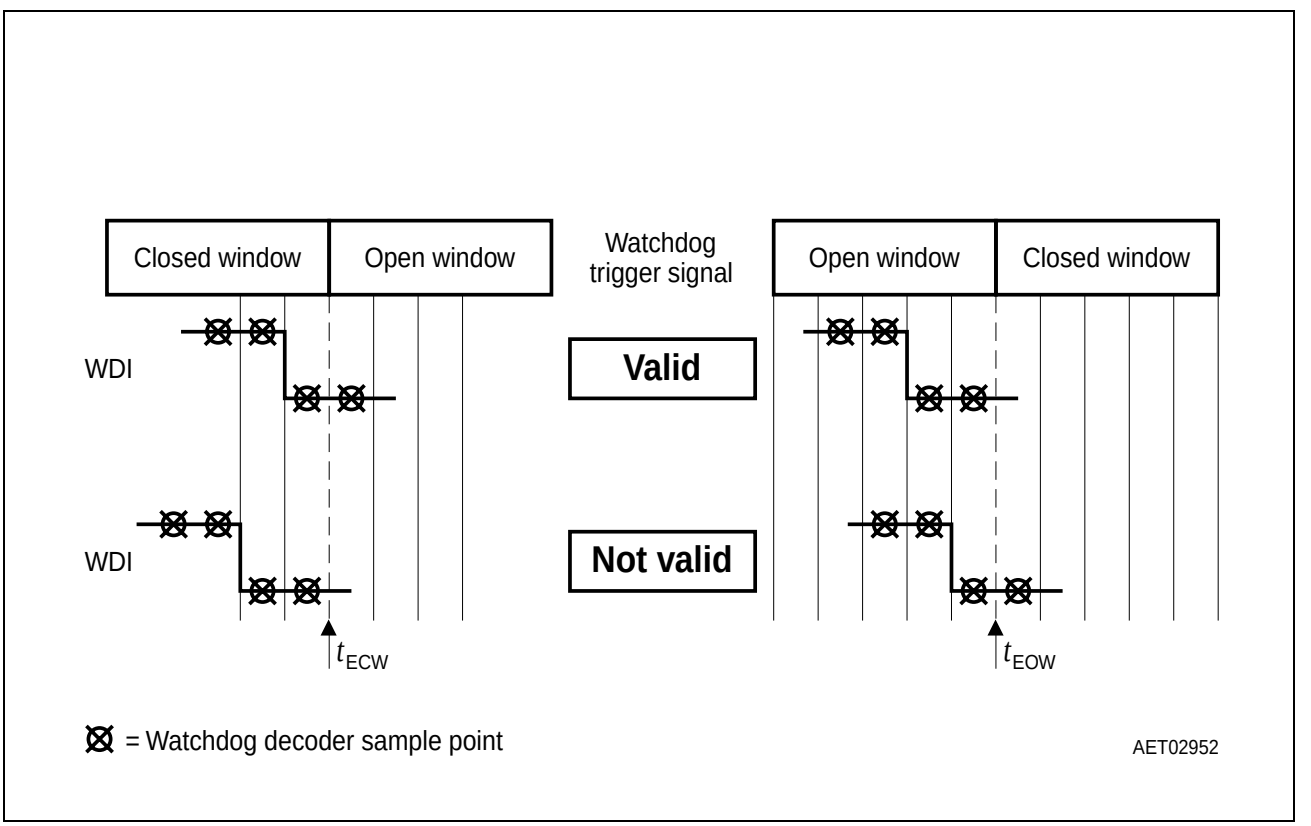
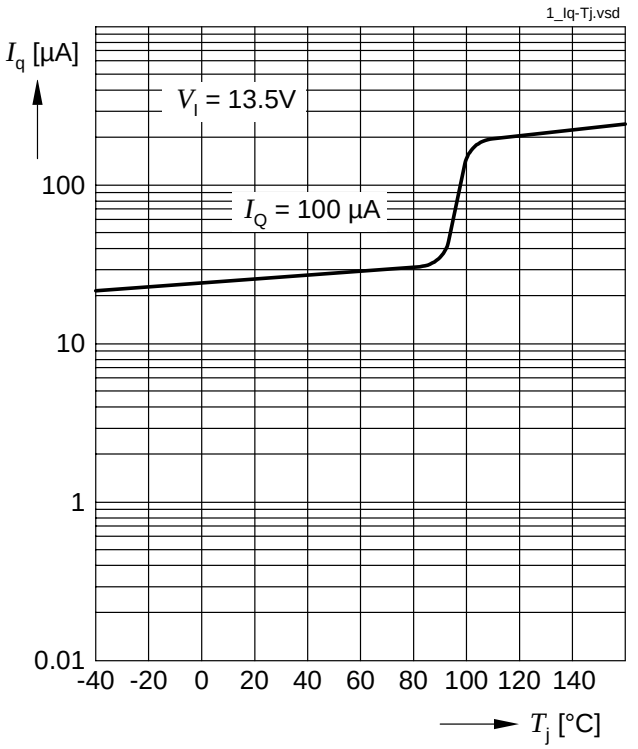


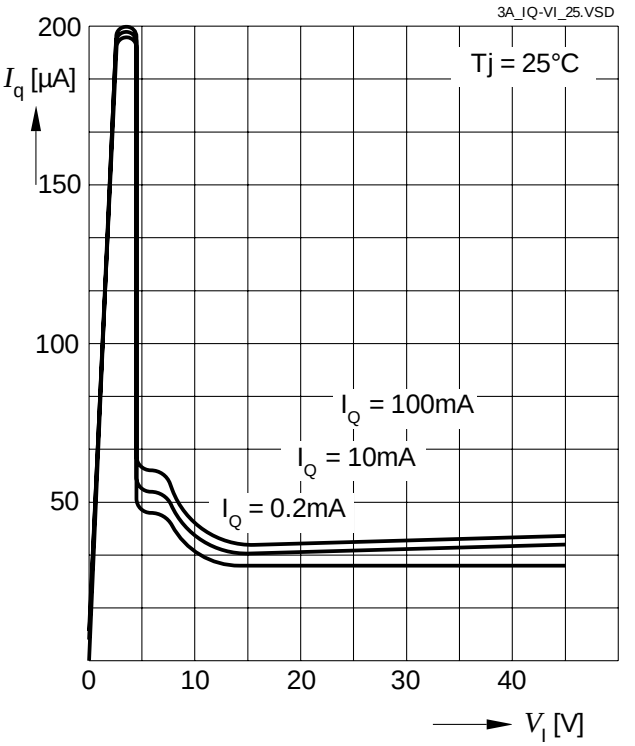
Figure 7 Window Watchdog Definitions

Typical Performance Characteristics

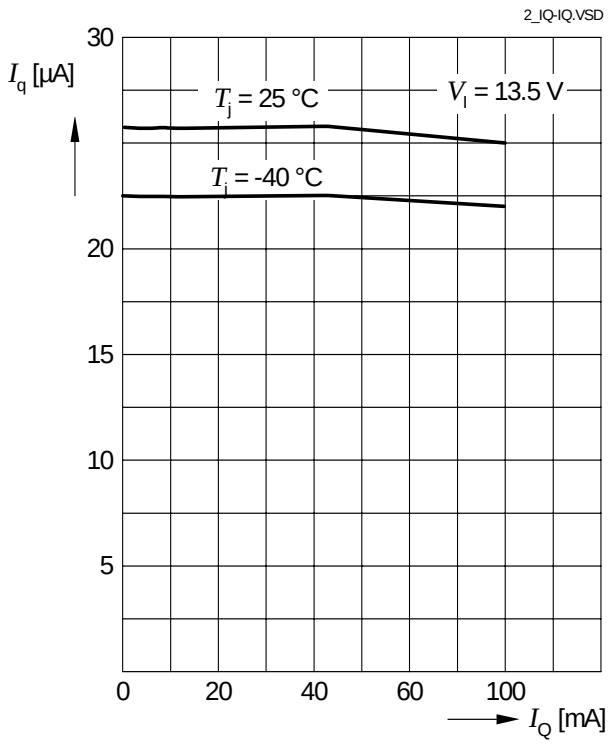
Current Consumption I_q versus Junction Temperature T_J (INH=ON)



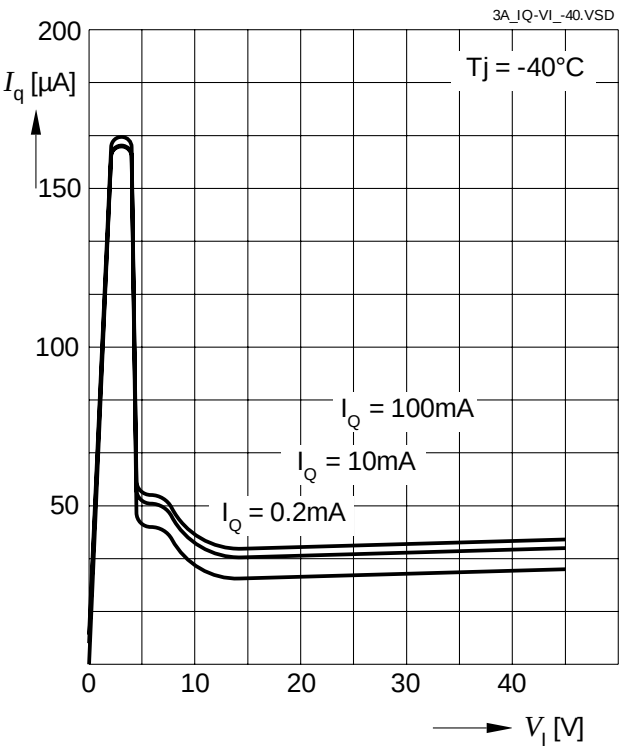
Current Consumption I_q versus Input Voltage V_I at T_J=25°C (INH=ON)



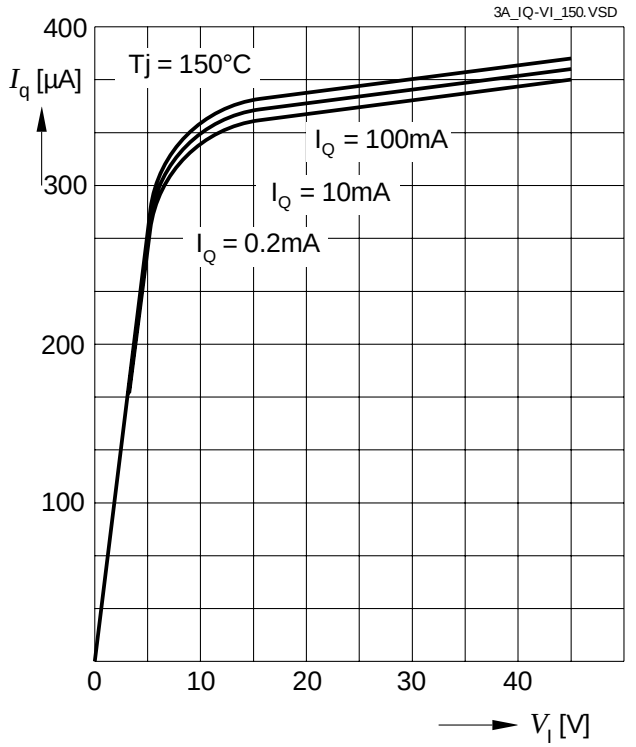
Current Consumption I_q versus Output Current I_Q (INH=ON)



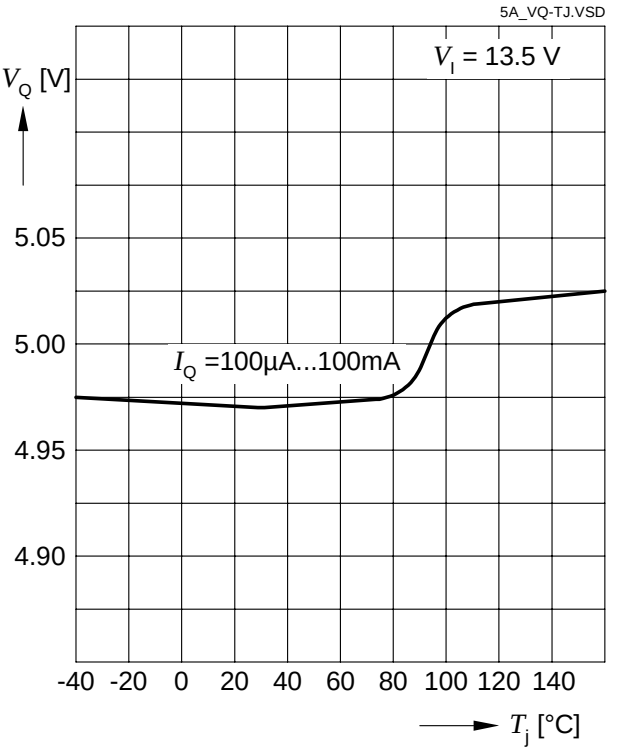
Current Consumption I_q versus Input Voltage V_I at T_J=-40°C (INH=ON)



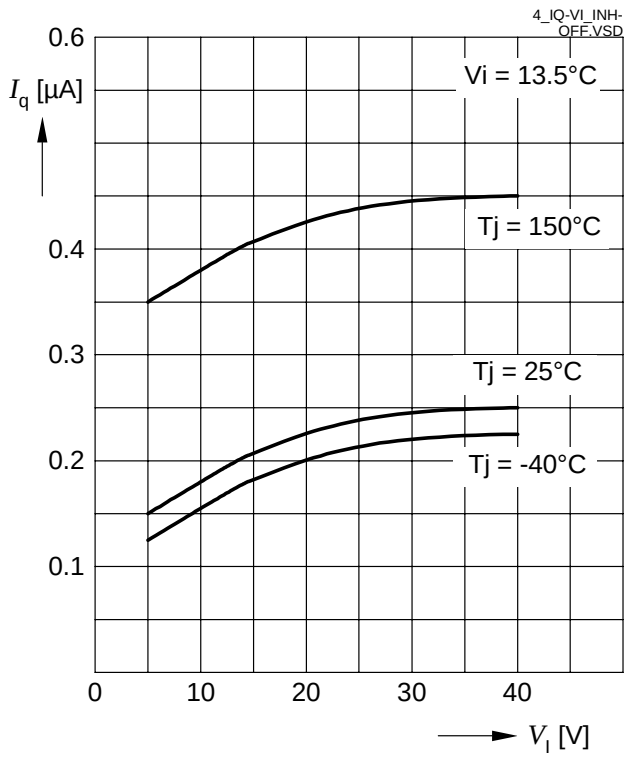
Current Consumption I_q versus Input Voltage V_I at T_J=150°C (INH=ON)



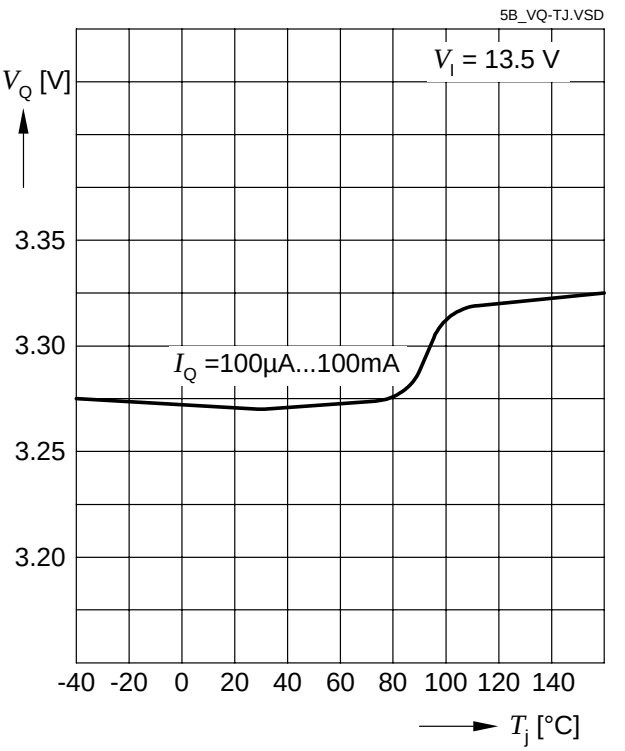
Output Voltage V_Q versus Junction Temperature T_J (5V Version)



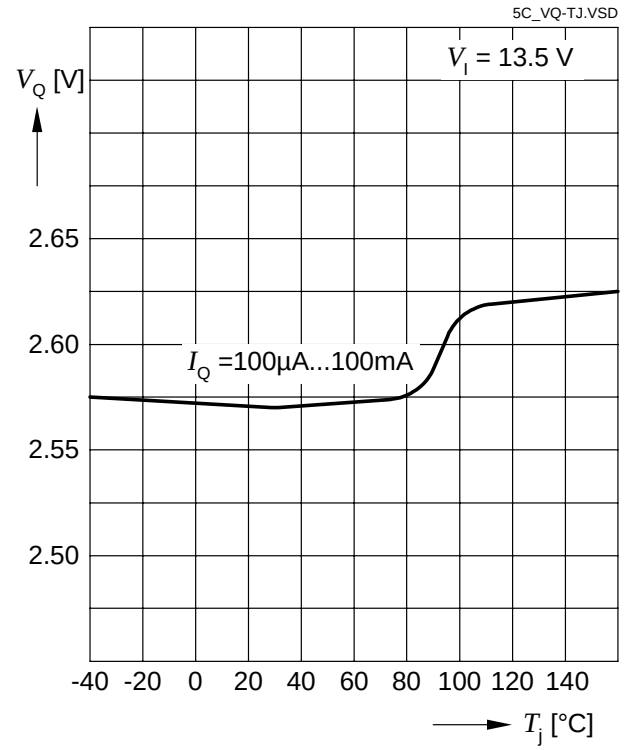
Current Consumption I_q versus Input Voltage V_I at T_J=150°C (INH=OFF)



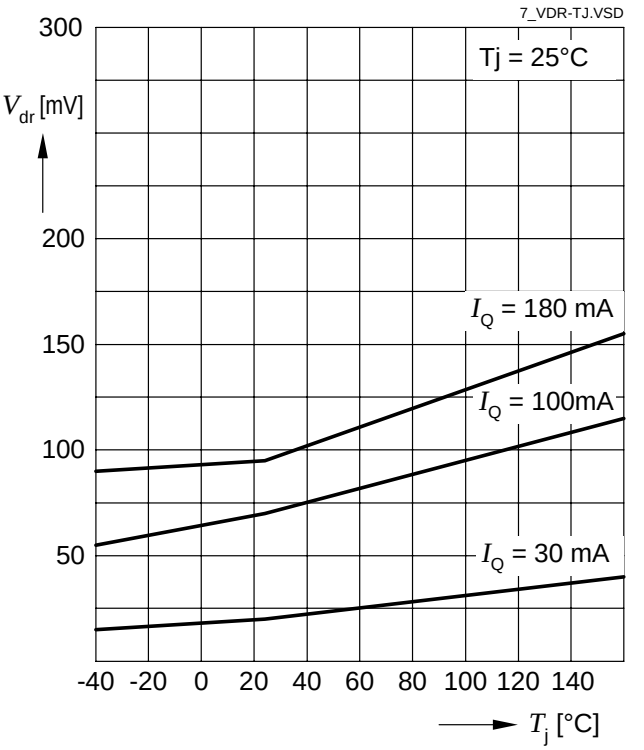
Output Voltage V_Q versus Junction Temperature T_J (3.3V Version)



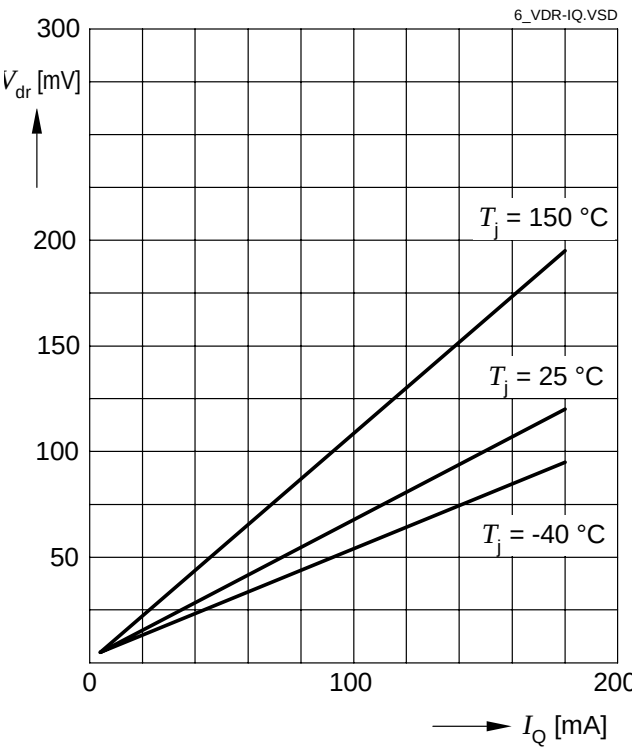
Output Voltage V_Q versus Junction Temperature T_J (2.6V Version)



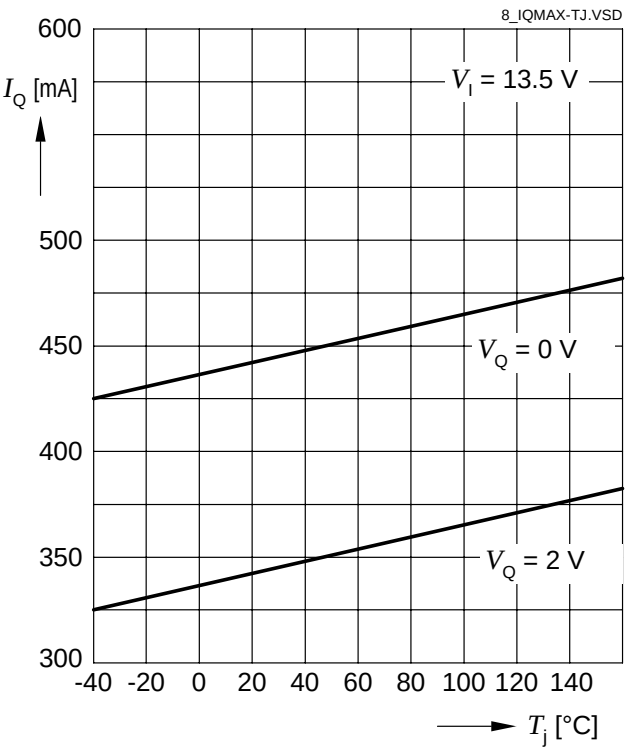
Dropout Voltage V_{dr} versus Junction Temperature T_J



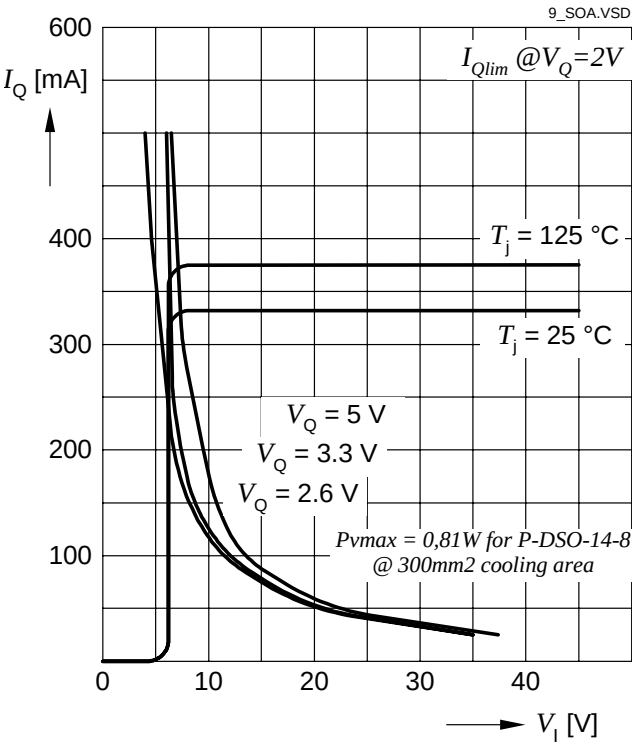
Dropout Voltage V_{dr} versus Output Current I_Q



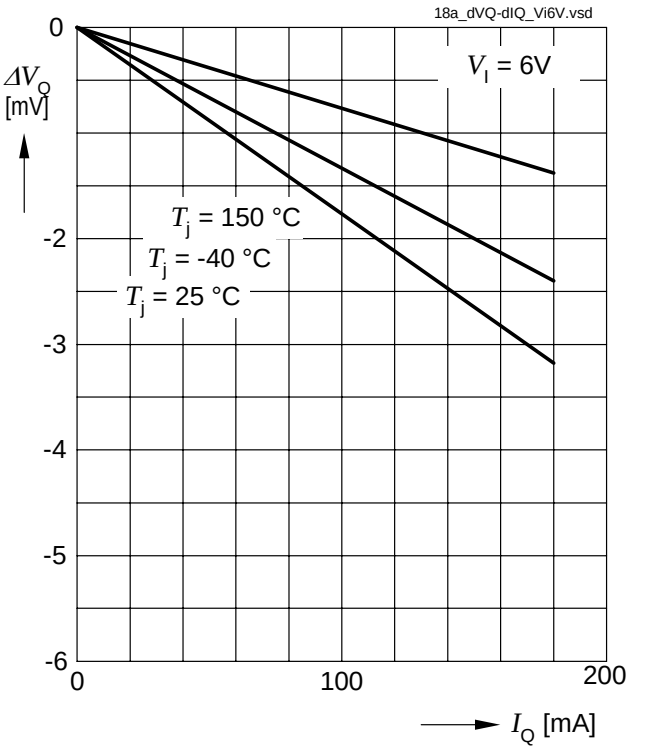
Maximum Output Current I_Q versus Junction Temperature T_J



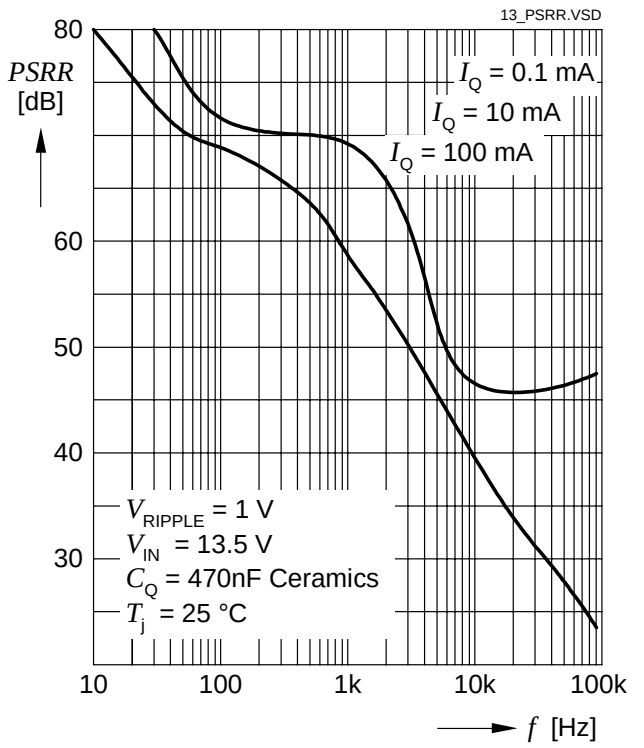
Maximum Output Current I_Q versus Input Voltage V_I



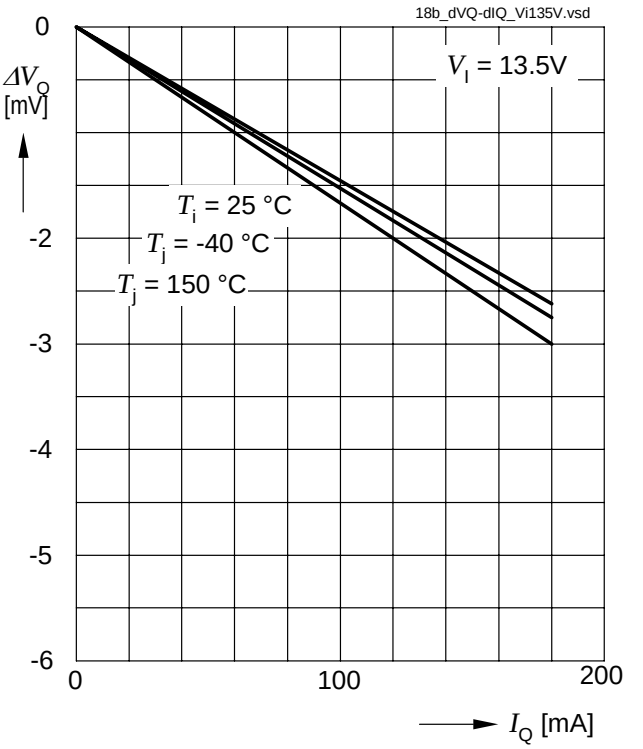
Load Regulation dV_Q versus Output Current Change dI_Q



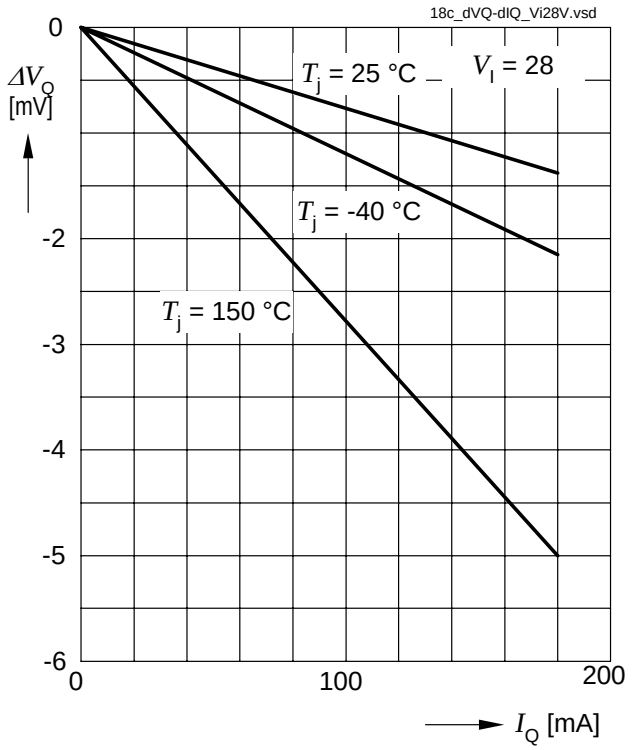
Power Supply Ripple Rejection PSRR



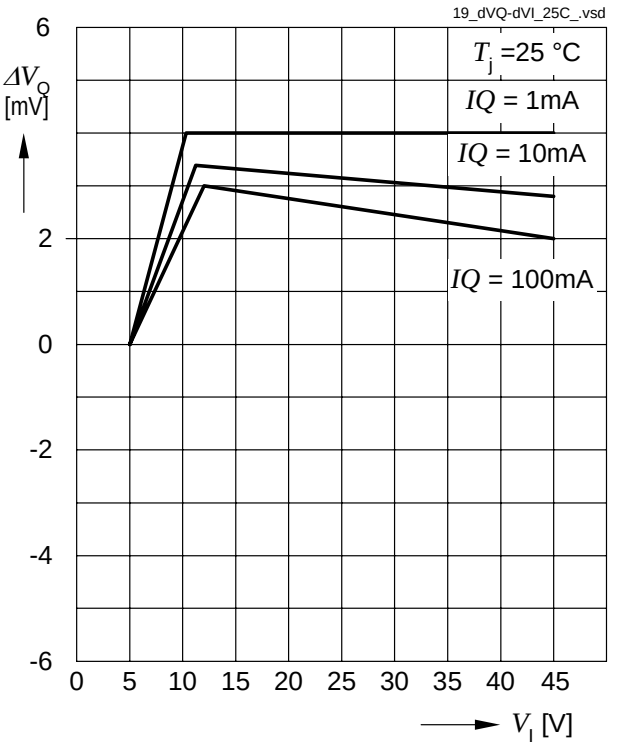
Load Regulation dV_Q versus Output Current Change dI_Q



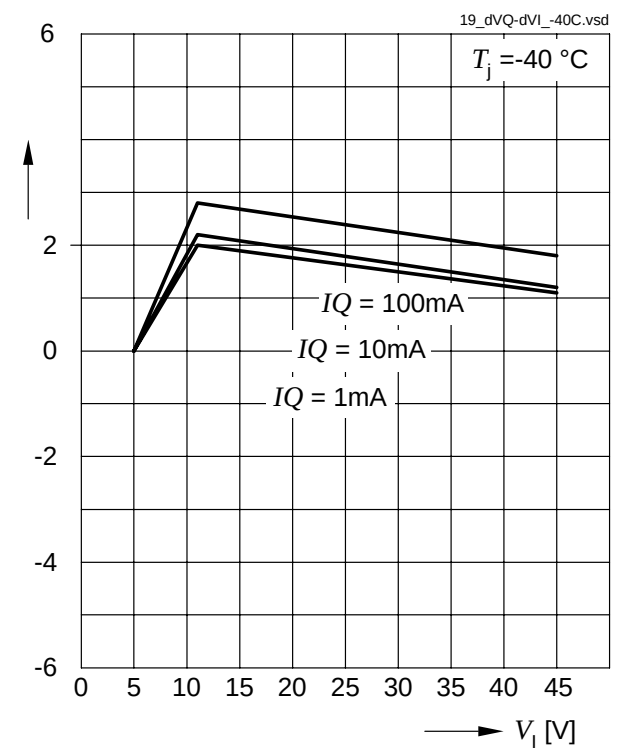
Load Regulation dV_Q versus Output Current Change dI_Q



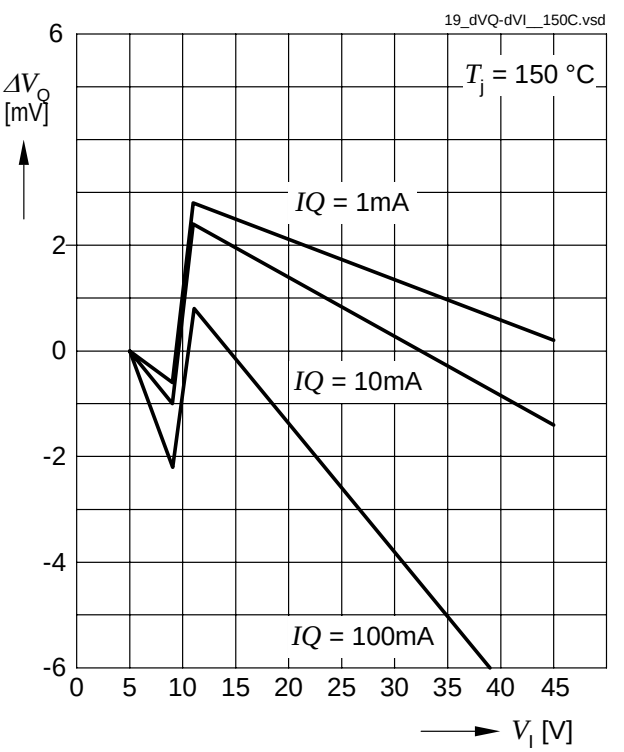
Line Regulation dV_Q versus Input Voltage Change dV_I



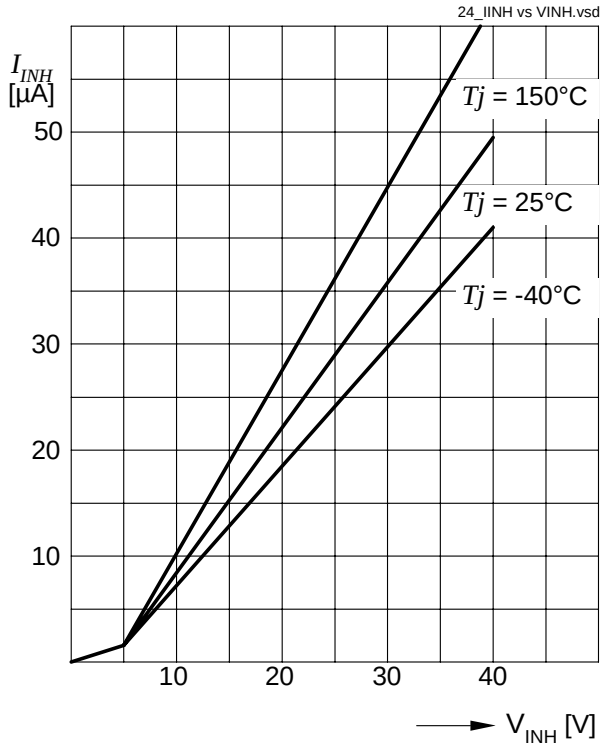
Line Regulation dV_Q versus Input Voltage Change dV_I



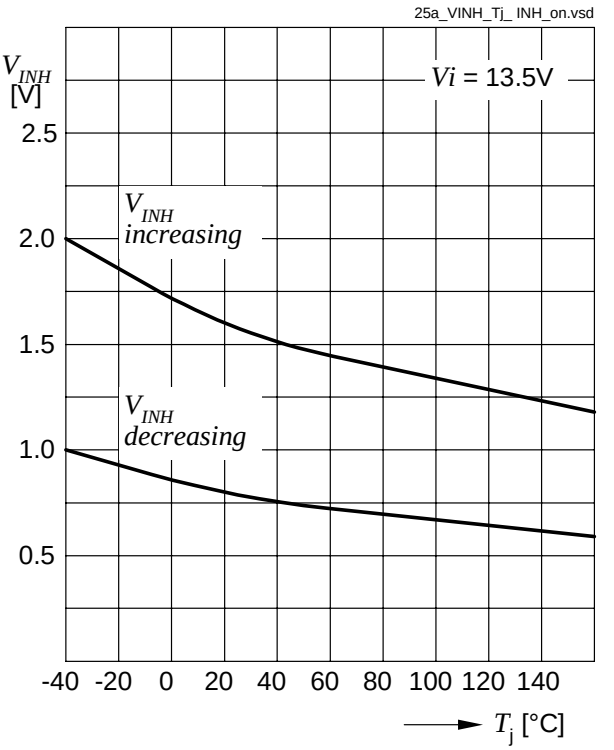
Line Regulation dV_Q versus Input Voltage ChangedV$_I$



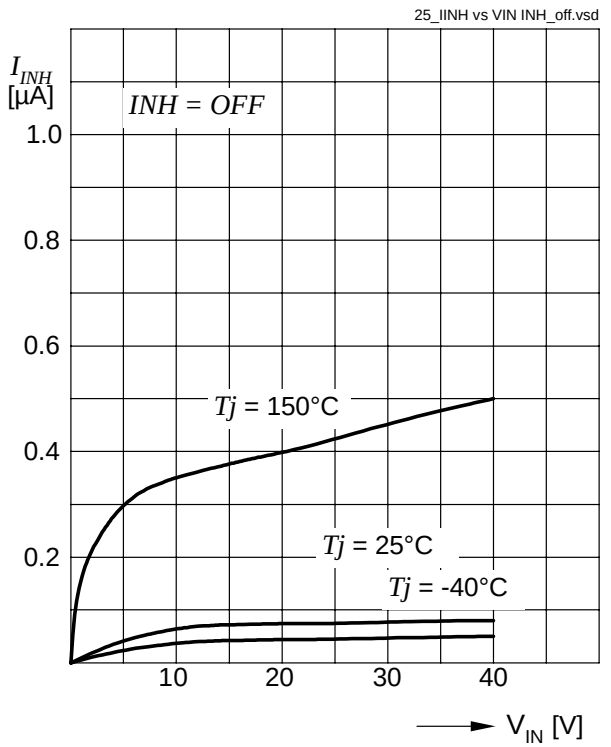
Inhibit Input Current I_{INH} versus Inhibit Input Voltage V_{INH}



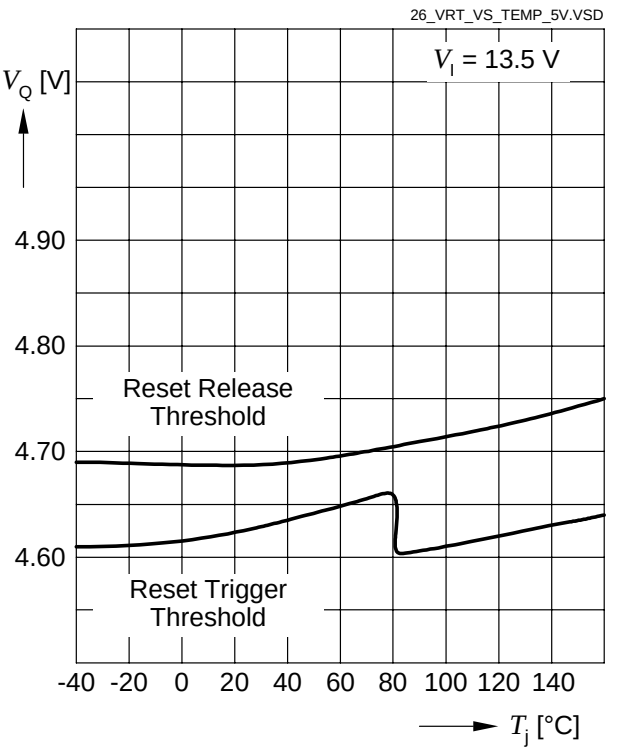
Inhibit Turn-ON/OFF Threshold V_{INH_ON} versus Junction Temperature T_J



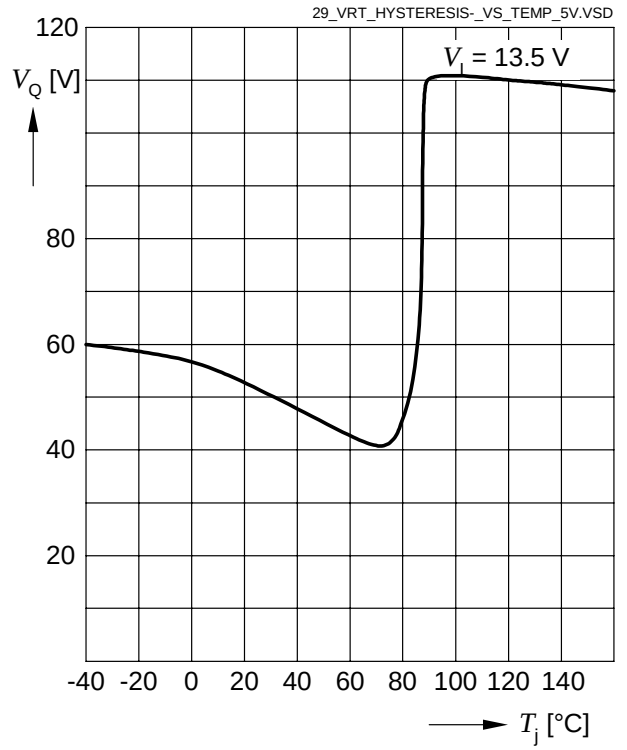
Inhibit Input Current I_{INH} versus Input Voltage V_i, INH=Off



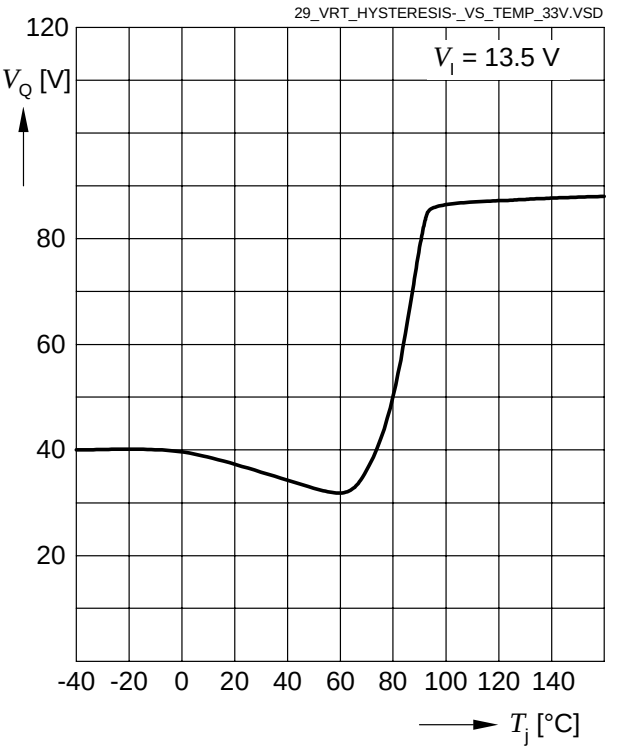
Reset Threshold V_{RT} versus Junction Temperature T_J (5V-Version)



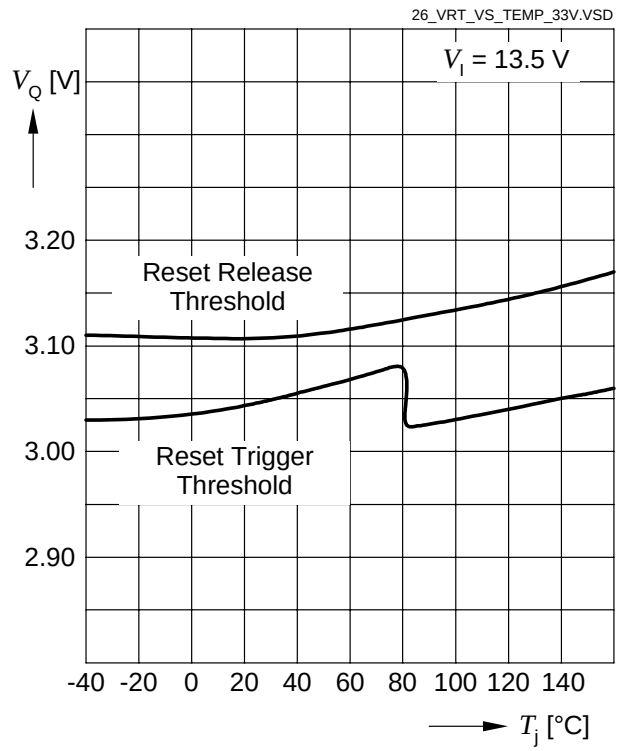
RReset Hysteresis versus Junction Temperature T_J (5V-Version)



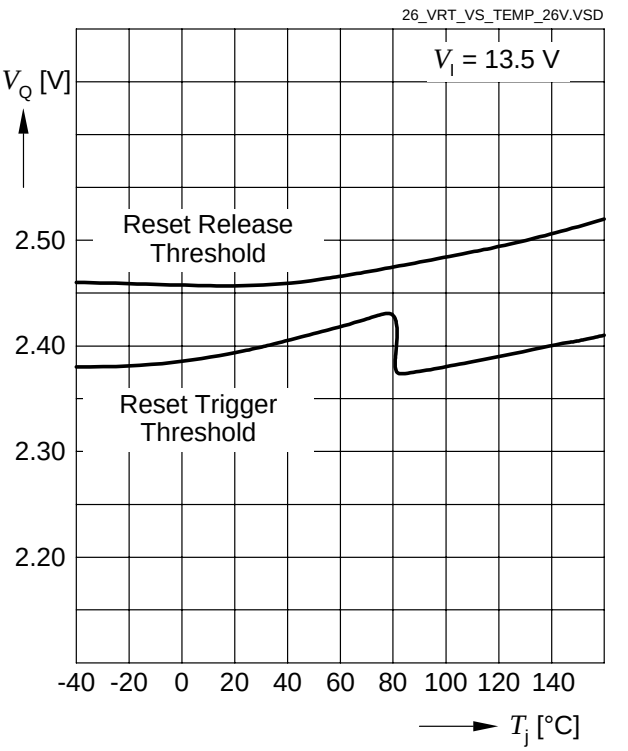
Reset Hysteresis versus Junction Temperature T_J (3.3V-Version)



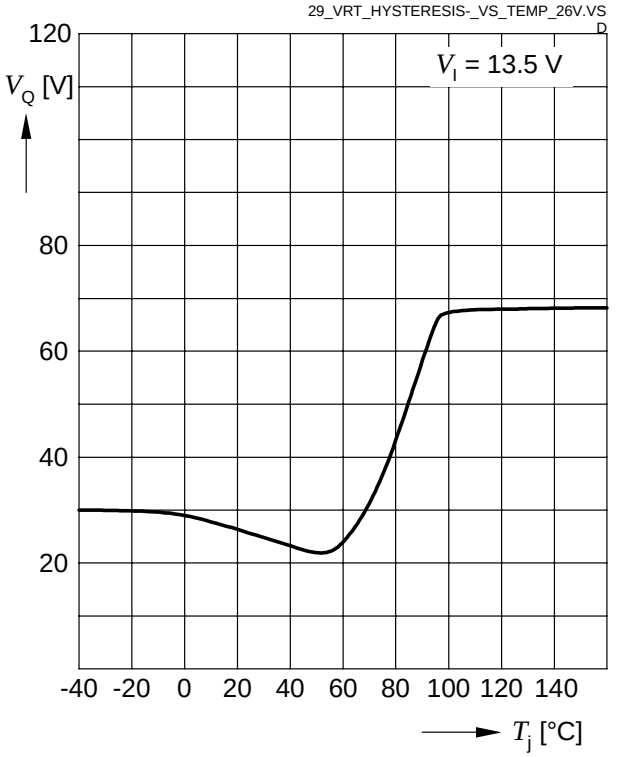
Reset Threshold V_{RT} versus Junction Temperature T_J (3.3V-Version)



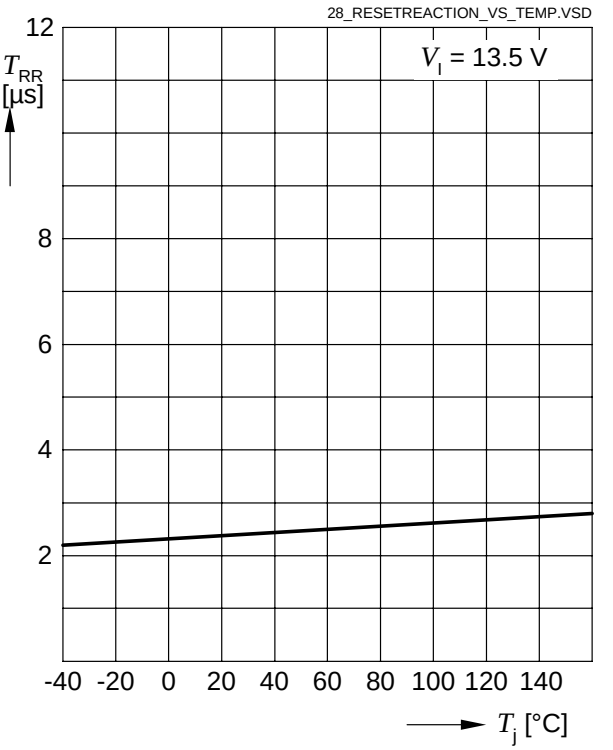
Reset Threshold V_{RT} versus Junction Temperature T_J (2.6V-Version)



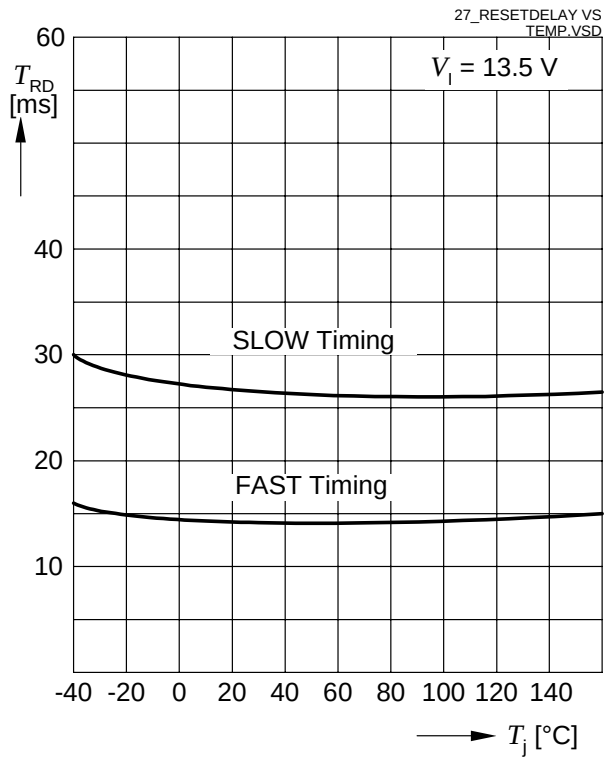
Reset Hysteresis versus Junction Temperature T_J (2.6V-Version)



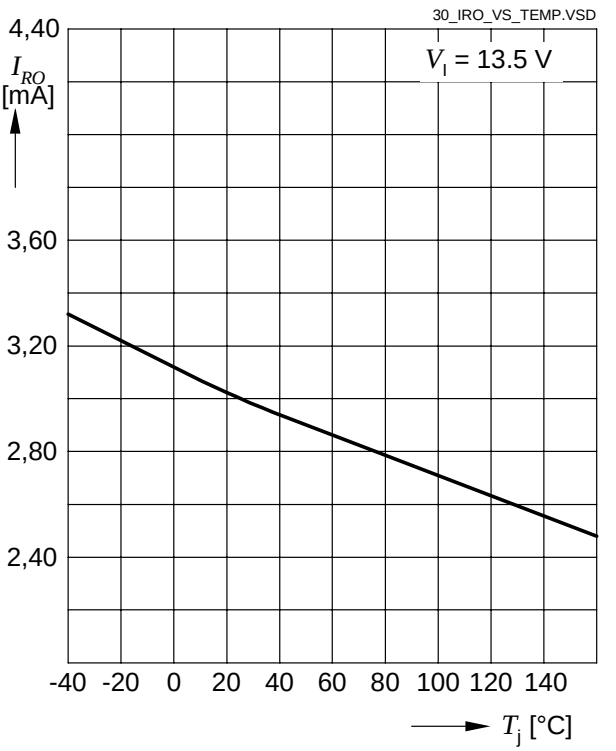
Reset Reaction Time T_{rr} versus Junction Temperature T_J



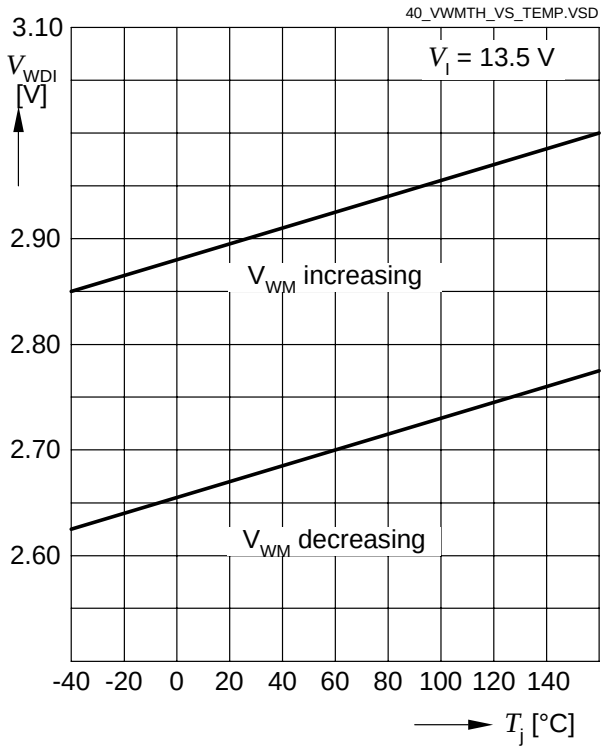
Reset Delay T_{RD} Time versus Junction Temperature T_J



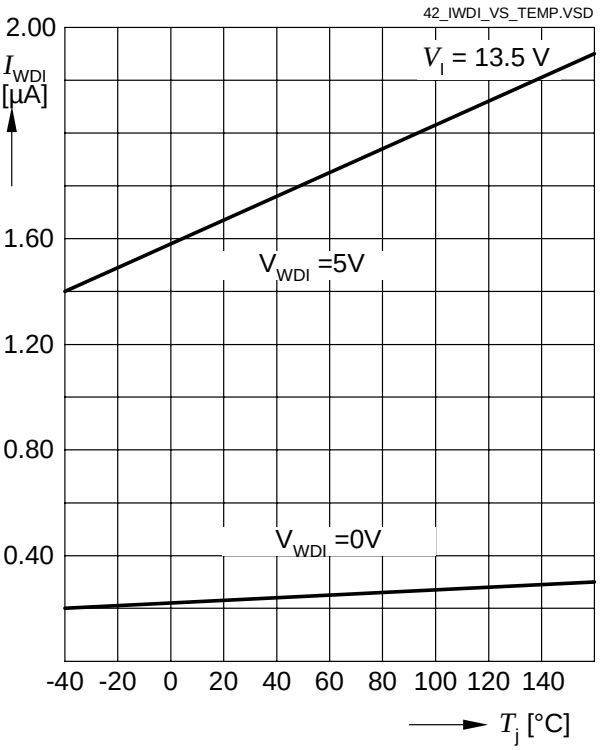
Reset Output Sink Current I_{RO} versus Junction Temperature T_J



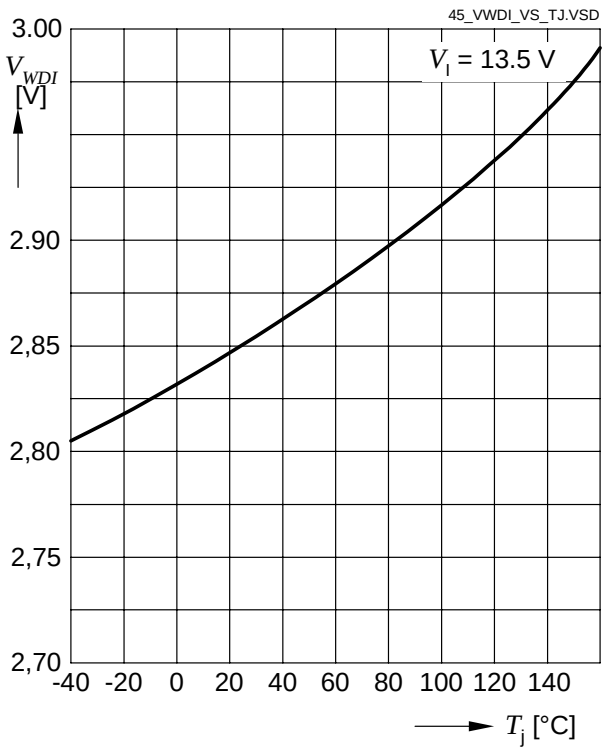
Watchdog Mode Bit Threshold V_{WM} versus Junction Temperature T_J



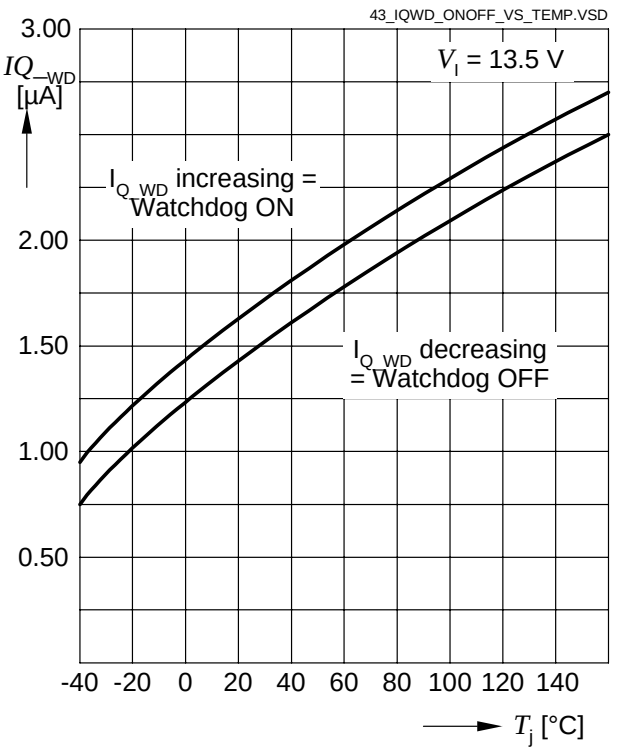
Watchdog Input Current I_{WDI} versus Junction Temperature T_J



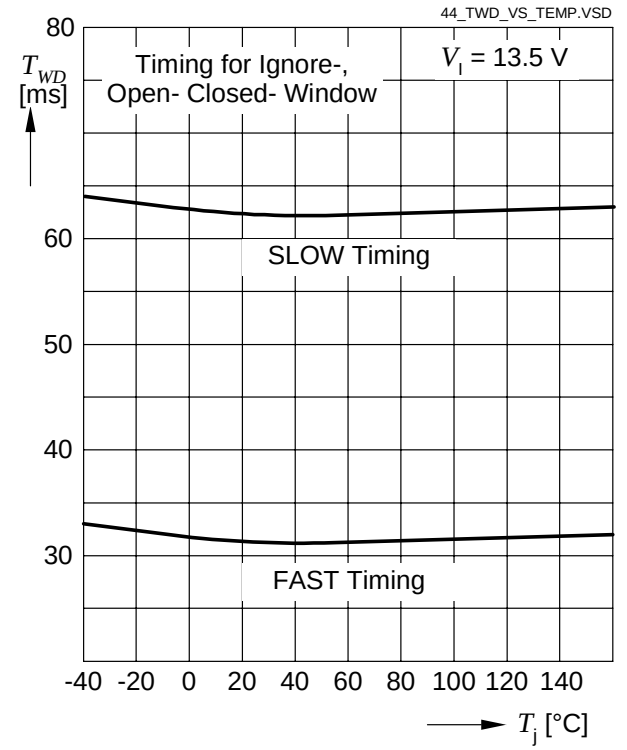
Watchdog Input Threshold V_{WDI} versus Junction Temperature T_J



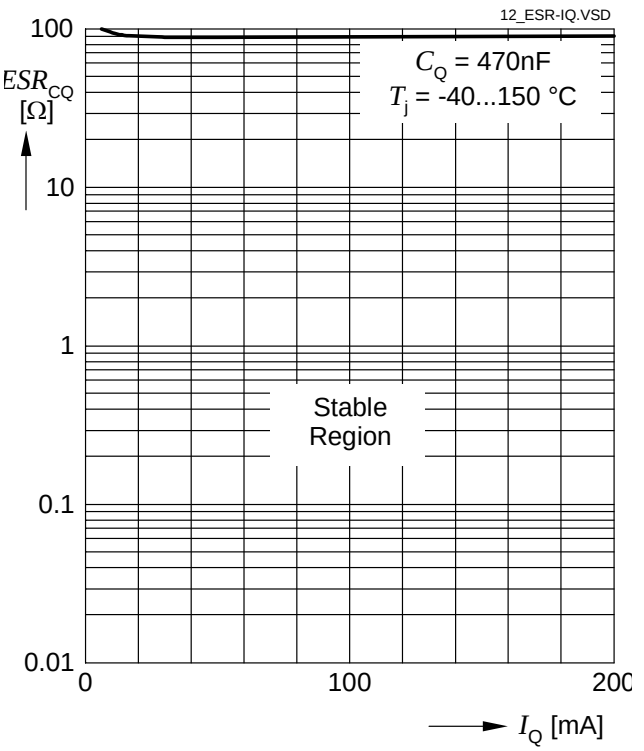
Watchdog Deactivation Current I_{Q_WD} versus Junction Temperature T_J



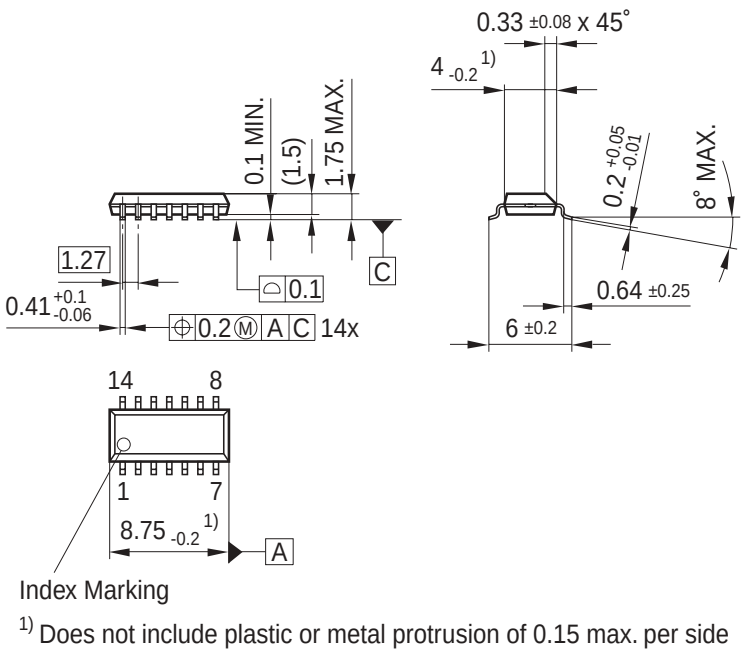
Watchdog Timing T_{WD} versus Junction Temperature T_J



Region of Stability



Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 1 Package Drawing P-DSO-14-8

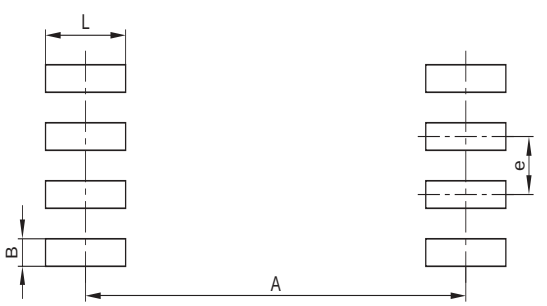


Figure 2 Foot Print for P-DSO-14-8
e=1.27 mm; A=5.69 mm; L=1.31 mm; B=0.65 mm

Remarks

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