SC1545-1.8
500mA SmartLDO™ With Power Up Signal Sequencing

POWER MANAGEMENT

Description

The SC1545 was designed for instantly available motherboard applications. As part of the Semtech family of SmartLDOs it provides additional control functions not available in a standard LDO.

The device provides the capability to control three separate supplies. There is an on-board 500mA, 1.8V LDO with current limit protection, and drive pins for an N-channel MOSFET and a P-channel MOSFET. Internal logic circuitry ensures that the system starts up in a controlled manner, and that the correct outputs are enabled during specific sequences of BF_CUT and SLP.

The LDO draws its power from the 5V standby supply, and the N-channel MOSFET drive is derived from the 12V supply.

The SC1545 is available in the surface mount SO-8 package.

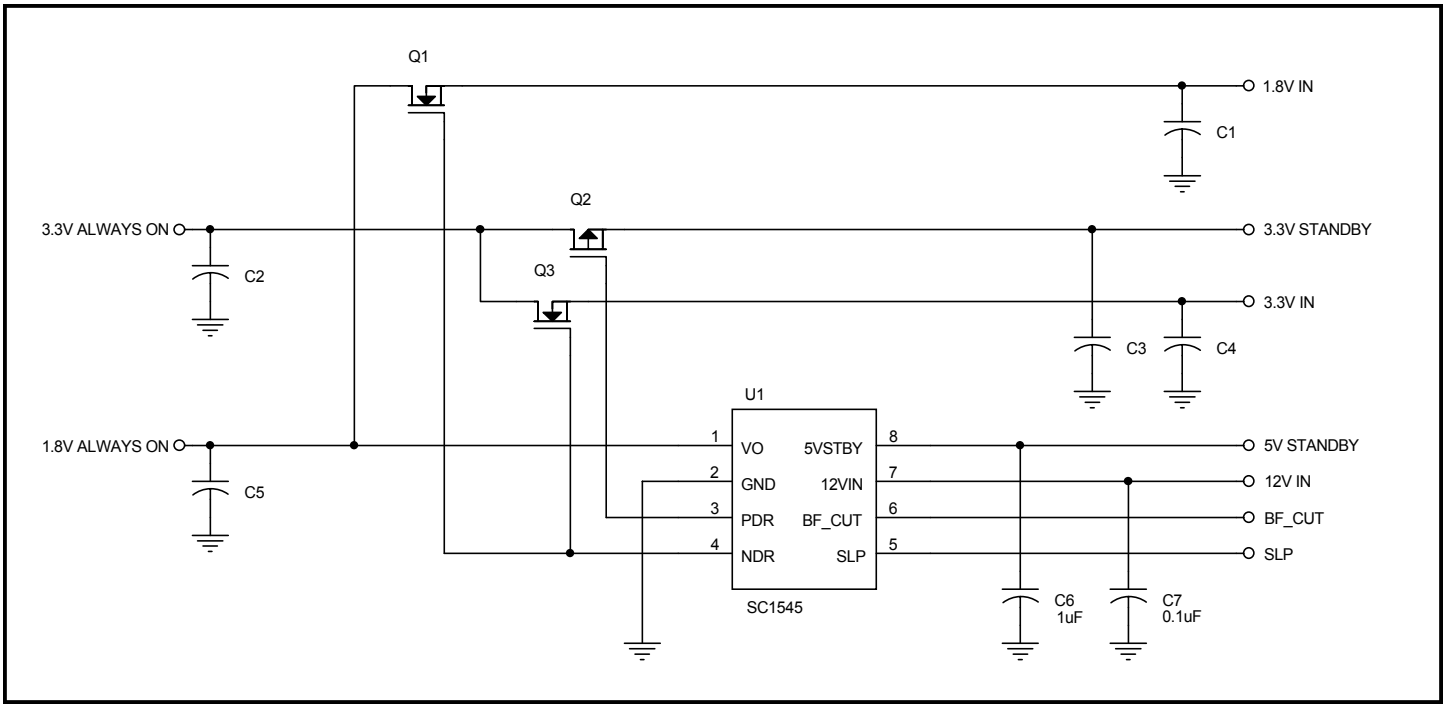
Features

- 500mA LDO with Over Current Protection (OCP)
- ±2% LDO regulation over line, load and temperature
- Power sequencing for three supplies
- Over temperature protection
- SO-8 surface mount package

Applications

- Instantly available motherboards
- Embedded systems
- Desktop computers

Typical Application Circuit



Notes:

(1) 1.8V Always On generated from SC1545 1.8V LDO and system 1.8V using one external N-channel MOSFET. MOSFET source connected to system 1.8V to prevent backfeeding through the body diode when this supply is low.
(2) 3.3V Always On generated from system 3.3V and 3.3V Standby supplies using two external MOSFETS, one N-channel and one P-channel. N-channel MOSFET source connected to sytem 3.3V to prevent backfeeding through the body diode when this supply is low.

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
12V Input Voltage Range	V_{12VIN}	-0.3 to +15	V
5V Input Voltage Range	V_{5VSTBY}	-0.3 to +7	V
P-channel MOSFET Gate Drive	V_{PDR}	-0.3 to 5VSTBY	V
N-channel MOSFET Gate Drive	V_{NDR}	-0.3 to 12VIN	V
Input Pins	V_{BF_CUT}, V_{SLP}	-0.3 to 5VSTBY	V
Thermal Impedance Junction to Ambient(1)	θ_{JA}	65	°C/W
Thermal Impedance Junction to Case	θ_{JC}	47	°C/W
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature Range	T_J	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Seconds	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	V_{ESD}	1	kV

Note: (1) 1 square inch of 1/16" FR-4, double sided, 1 oz. minimum copper weight.

Electrical Characteristics

Unless specified: V_{12VIN} = 12V, V_{5VSTBY} = 5V, C_{OUT} = 100µF, T_A = 25°C. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
12VIN						
Supply Voltage	V_{12VIN}		**11.28**	12.00	**12.72**	V
Quiescent Current	I_{Q12}			800	1100	µA
					1300	
5VSTBY						
Supply Voltage	V_{5VSTBY}		4.7	5.0	**5.3**	V
Quiescent Current	I_{Q5}	LDO ON		9.5	11.0	mA
					12.0	
		LDO OFF		3	4	mA
					5	
Undervoltage Lockout (5VSTBY)						
UVLO Threshold	V_{UVLO}	V_{5VSTBY} rising	**4.1**	4.3	**4.5**	V
		V_{5VSTBY} falling	**3.9**	4.1	**4.3**	V

Electrical Characteristics (Cont.)

Unless specified: V_{12VIN} = 12V, V_{5VSTBY} = 5V, C_{OUT} = 100µF, T_A = 25°C. Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Undervoltage Lockout (5VSTBY) (Cont.)						
Hysteresis	V_{HYST}			200		mV
Logic Reset Threshold	V_{RST}		**1.5**	2.0	**2.5**	V
OUT						
LDO Output Voltage	V_{OUT}	4.7V ≤ V_{5VSTBY} ≤ 5.3V, 1mA ≤ I_{OUT} ≤ 500mA	-1.0% **-2.0%**	1.8	+1.0% **+2.0%**	V
LDO Output Voltage(1) During Load Transients	$V_{OUT(T)}$	I_{OUT} = 0mA to 500mA, t_r = 8A/µs max.	**-3.0%**	1.8	**+3.0%**	V
Time to Regulation(2)	t_{REG}				**5**	µs
Inputs (BF_CUT & SLP)						
Input Resistance	R_{IN}	V_{BF_CUT} = V_{SLP} = 5V	**1**	10		MΩ
High Level Input Voltage	V_{IH}		**2.0**			V
Low Level Input Voltage	V_{IL}				**0.8**	V
NDR						
Peak Drive Current	$I_{NDR(PK)}$	Sinking: V_{NDR} = 0.5V; Sourcing: V_{NDR} = 10V	**25**			mA
Output Voltage	$V_{OH(N)}$	Full ON, I_{NDR} = 100µA	**10**	12		V
	$V_{OL(N)}$	Full OFF, I_{NDR} = -100µA			**0.3**	
Drive Low Delay	$t_{DL(N)}$	Measured from BF_CUT threshold to 90% of NDR			**200**	ns
Fall Time	$t_{f(N)}$	Measured from 90% to 10% of NDR			**1.2**	µs
Drive High Delay	$t_{DH(N)}$	Measured from BF_CUT/SLP threshold to 10% of NDR			**350**	ns
Rise Time	$t_{r(N)}$	Measured from 10% to 90% of NDR			**1.2**	µs
PDR						
Peak Drive Current	$I_{PDR(PK)}$	Sinking: V_{PDR} = 0.5V; Sourcing: V_{PDR} = 3.5V	**25**			mA
Output Voltage	$V_{OH(P)}$	Full OFF, I_{PDR} = 100µA	**4**	5		V
	$V_{OL(P)}$	Full ON, I_{PDR} = -100µA			**0.3**	
Drive Low Delay	$t_{DL(P)}$	Measured from BF_CUT threshold to 90% of PDR			**200**	ns
Fall Time	$t_{f(P)}$	Measured from 90% to 10% of PDR			**1.2**	µs
Drive High Delay	$t_{DH(P)}$	Measured from BF_CUT/SLP threshold to 10% of PDR			**350**	ns
Rise Time	$t_{r(P)}$	Measured from 10% to 90% of PDR			**1.2**	µs
Overcurrent Protection						
Current Limit	I_{CL}	V_{OUT} = 0V	**550**			mA

Electrical Characteristics (Cont.)

Notes:

(1) The LDO will bring the output back to within the regular V_{OUT} limits in less than 10µs.

(2) External 1.8V ± 2% applied at output, turning off when NDR goes low. C_{OUT} = 100µF to 400µF, I_{OUT} = 50mA to 200mA.

(3) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Timing Diagrams

Power-up signal sequencing is shown in Figure 1 below. BF_CUT, PDR and NDR follow the power rails up to their final values. SLP goes to its high value when the power rails have stabilized, ~25msec after power on. BF_CUT is pulled low a period T1 after SLP goes high. T1 can be as short as 1ms but typical measured values are ~200ms. The 1.8V LDO output stays OFF through this entire sequence.

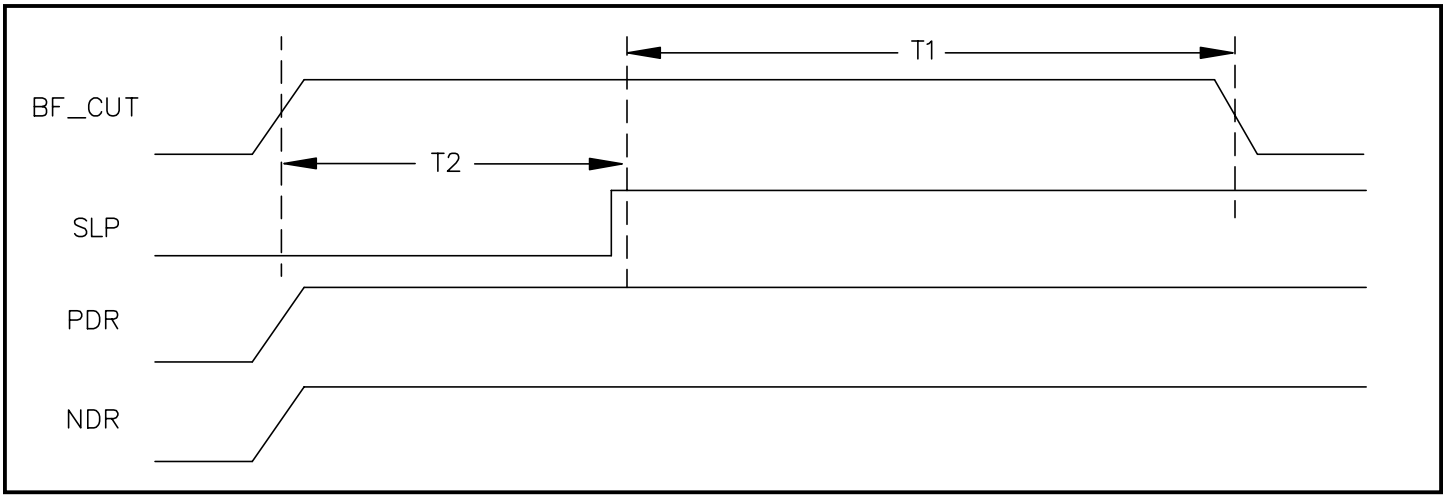


Figure 1: Power Up Signal Sequencing

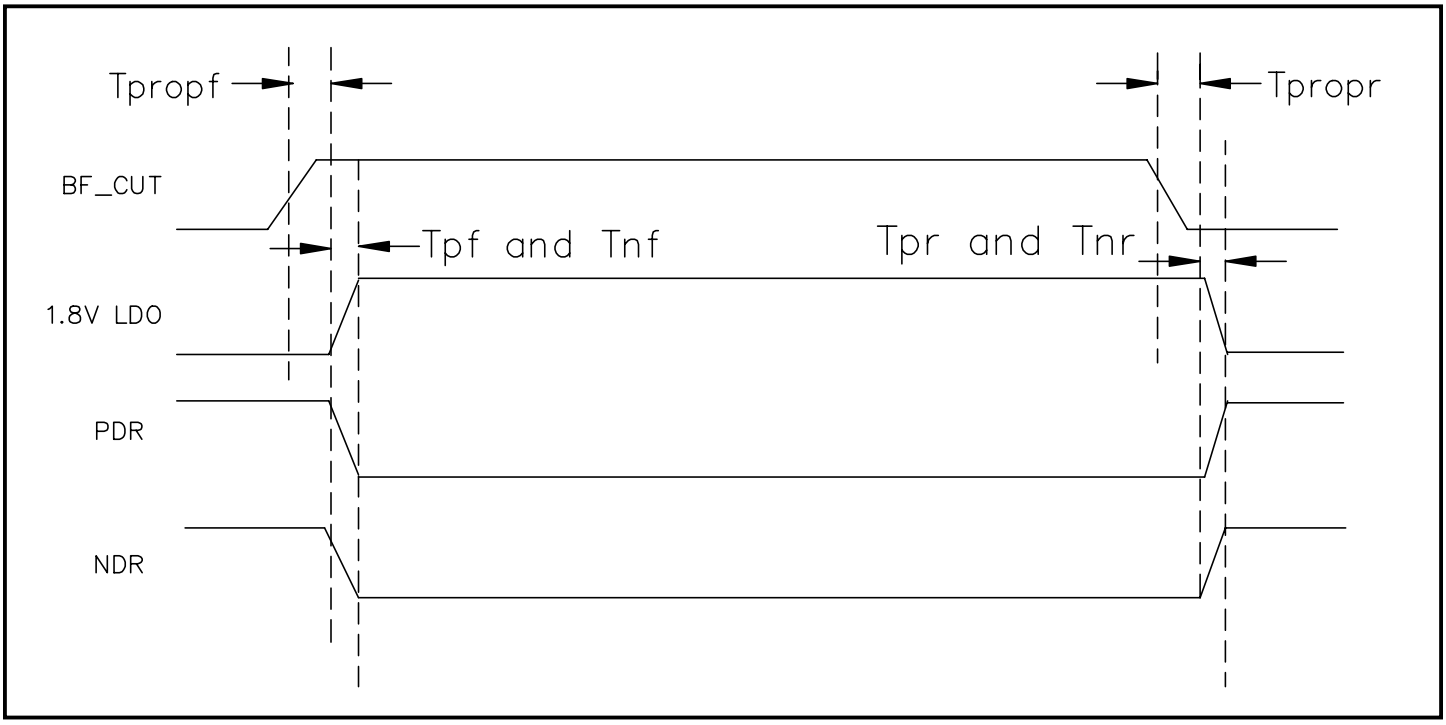


Figure 2: 1st Timing Sequence

Timing Diagrams (Cont.)

After power up, there are two possible signal sequences that the device will see. The first sequence is with SLP staying HIGH and BF_CUT transitioning from LOW to HIGH, remaining HIGH for an undetermined period and then going back to LOW. At this point, the system state is back to where it was at the end of the power up sequence. The sequence is shown in Figure 2 on page 4.

During these BF_CUT transitions, the propagation delays, rise and fall times, and going into regulation times for PDR, NDR and VO are described in the Electrical Characteristics on pages 2 and 3. The first sequence can start at any time after the end of the power up sequence.

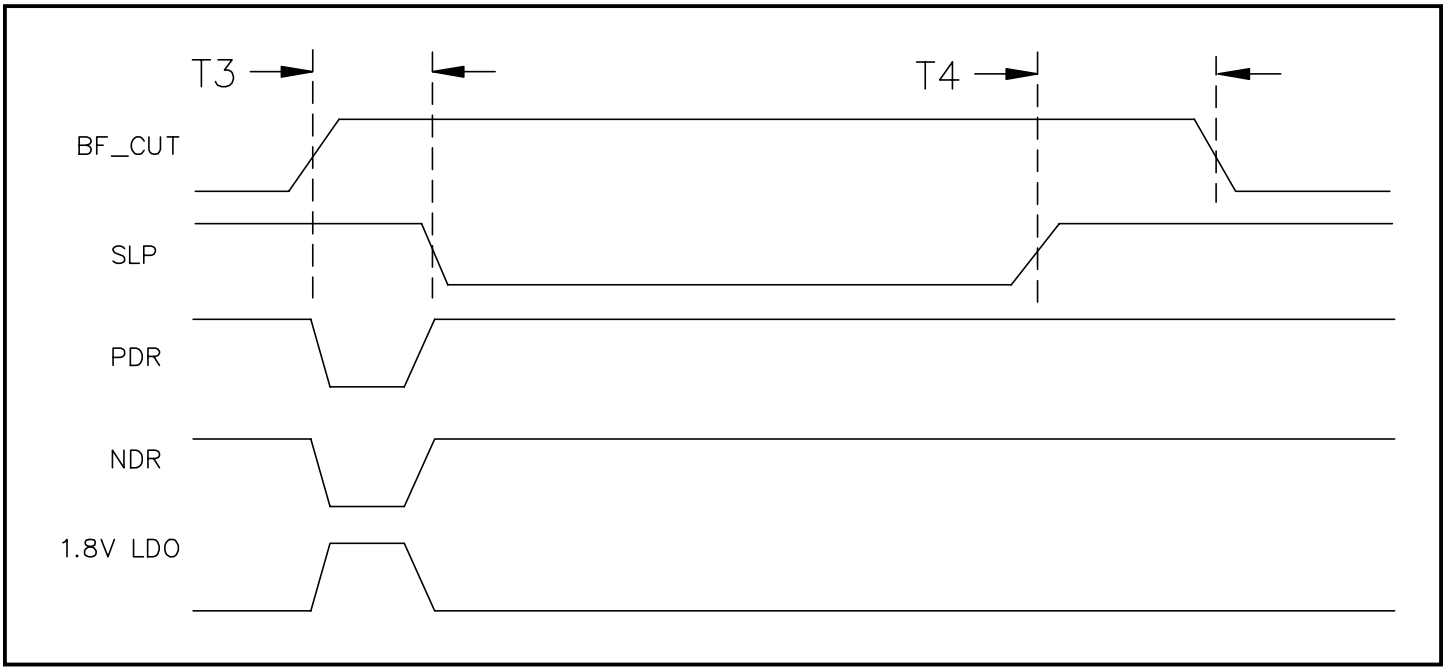
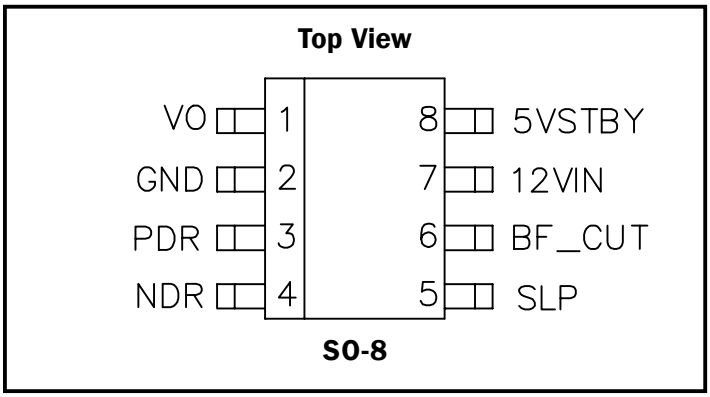


Figure 3: 2nd Timing Sequence

Signal sequencing for the second possible sequence is shown in Figure 3 above. BF_CUT goes from LOW to HIGH and SLP goes from HIGH to LOW, 30µsec to 65µsec (T3) later. When BF_CUT goes HIGH, PDR and NDR go LOW and the 1.8V LDO turns ON. When SLP goes LOW, PDR and NDR return to HIGH and the 1.8V LDO turns OFF. BF_CUT will stay HIGH and SLP will stay low for an undetermined time, after which SLP will go HIGH. A minimum of 1msec (T4) later, BF_CUT will go LOW and the system is back at the end of the power up sequence. Typical measured values of T4 are ~250msec. During all transitions, the propagation delays, rise and fall times, and going into regulation times for PDR, NDR and 1.8V LDO are described in the Electrical Characteristics on pages 2 and 3. The second sequence can start at any time after the end of the power up sequence.

Pin Configurations

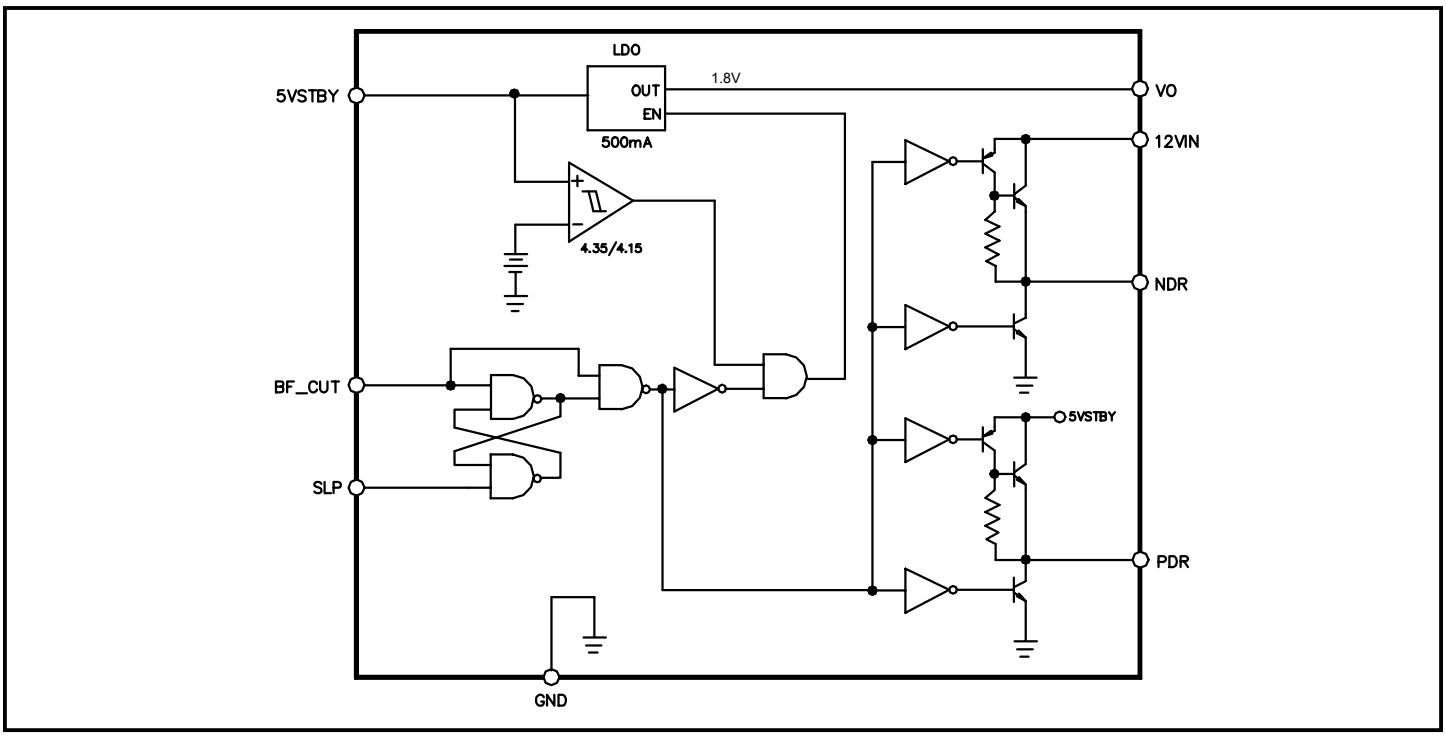


Ordering Information

Part Number[1]	Package
SC1545CS-1.8TR	SO-8

Note:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.

Block Diagram

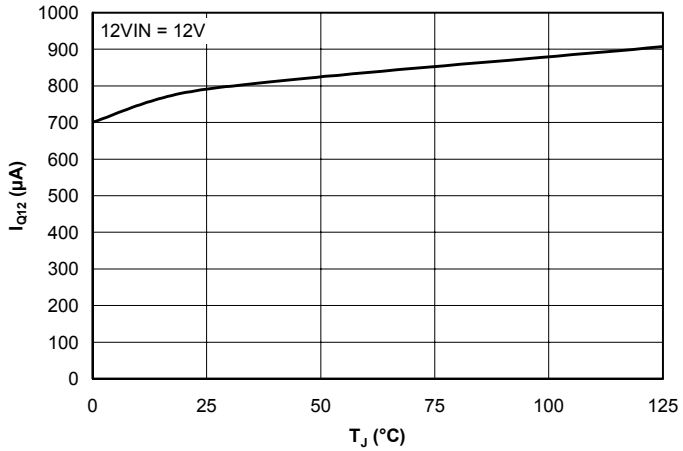


Pin Descriptions

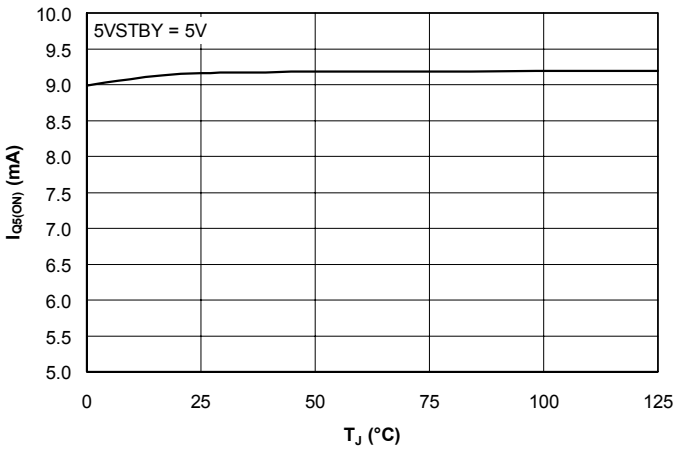
Pin	Pin Name	Pin Function
1	VO	LDO 1.8V output.
2	GND	Logic and power ground.
3	PDR	Gate drive signal for P-channel MOSFETs.
4	NDR	Gate drive signal for N-channel MOSFETs.
5	SLP	Control input #1.
6	BF_CUT	Control input #2.
7	12VIN	+12V input supply. Used for generating NDR only.
8	5VSTBY	+5V input supply.

Typical Characteristics

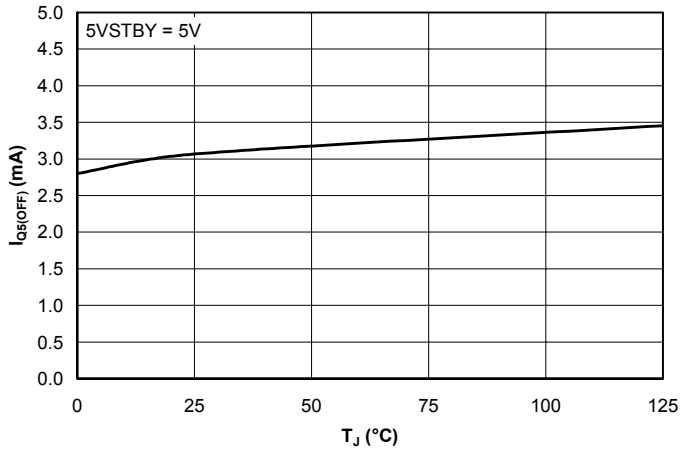
12VIN Quiescent Current vs. Junction Temperature



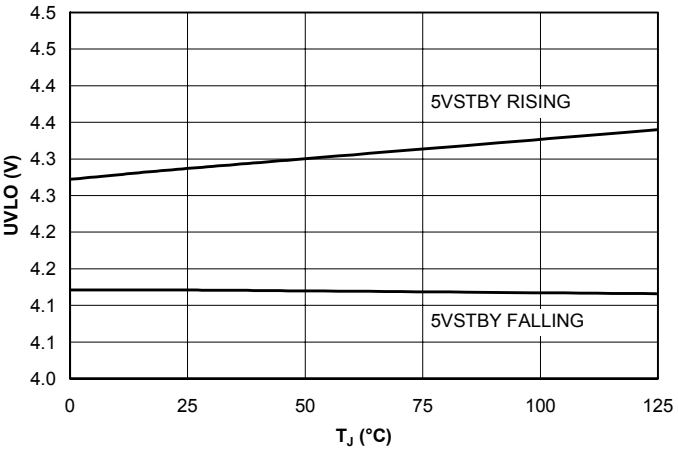
5VSTBY Quiescent Current (ON) vs. Junction Temperature



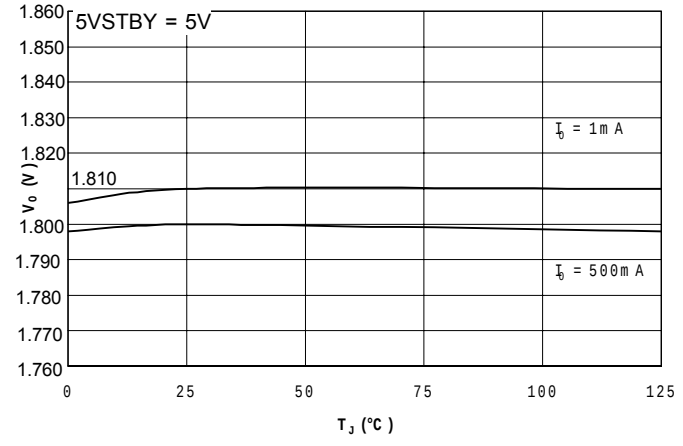
5VSTBY Quiescent Current (OFF) vs. Junction Temperature



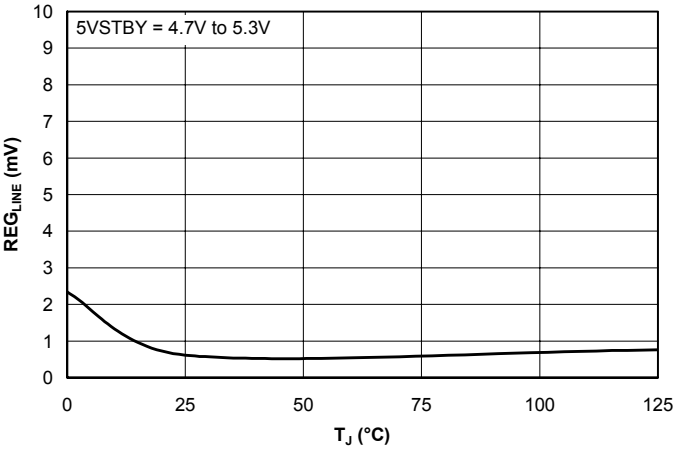
5VSTBY Under Voltage Lockout vs. Junction Temperature



LDO Output Voltage vs. Junction Temperature



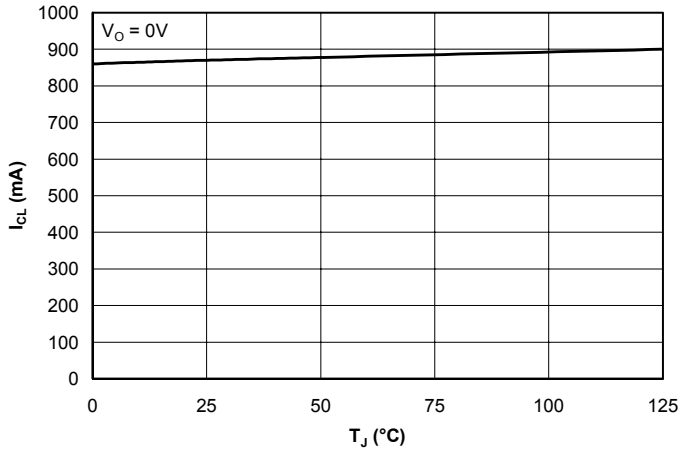
LDO Line Regulation vs. Junction Temperature



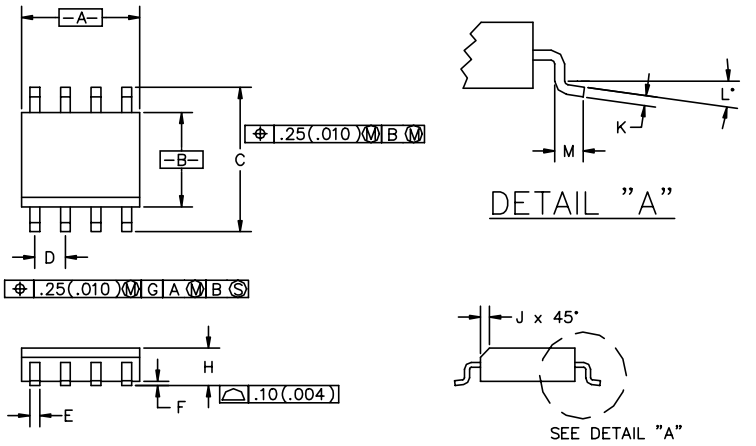
Typical Characteristics (Cont.)

LDO Current Limit vs.

Junction Temperature



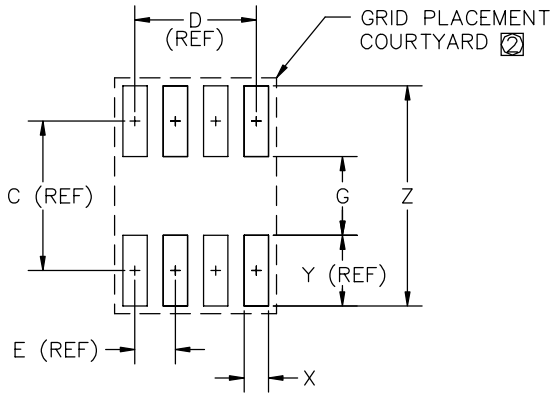
Outline Drawing - SO-8



JEDEC REF: MS-012AA

DIMENSIONS					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.188	.197	4.80	5.00	
B	.149	.158	3.80	4.00	
C	.228	.244	5.80	6.20	
D	.050 BSC		1.27 BSC		
E	.013	.020	0.33	0.51	
F	.004	.010	0.10	0.25	
H	.053	.069	1.35	1.75	
J	.011	.019	0.28	0.48	
K	.007	.010	.19	.25	
L	0°	8°	0°	8°	
M	.016	.050	0.40	1.27	

Land Pattern - SO-8



DIMENSIONS (1)					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	–	.19	–	5.00	–
D	–	.15	–	3.81	–
E	–	.05	–	1.27	–
G	.10	.11	2.60	2.80	–
X	.02	.03	.60	.80	–
Y	–	.09	–	2.40	–
Z	–	.29	7.20	7.40	–

(2) GRID PLACEMENT COURTYARD IS 12x16 ELEMENTS (6 mm X 8mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN IEC PUBLICATION 97.

(1) CONTROLLING DIMENSION: MILLIMETERS

Contact Information

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