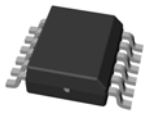
# VND7050AJ12-E

## Double channel high-side driver with CurrentSense analog feedback for automotive applications

**Datasheet - production data**



PowerSSO-12

## Features

| | | |
|---|---|---|
| Max transient supply voltage | $V_{CC}$ | 40 V |
| Operating voltage range | $V_{CC}$ | 4 to 28 V |
| Typ. on-state resistance (per Ch) | $R_{ON}$ | 50 mΩ |
| Current limitation (typ) | $I_{LIMH}$ | 30 A |
| Standby current (max) | $I_{STBY}$ | 0.5 µA |

- Automotive qualified
- General
  - Double channel smart high side driver with CurrentSense analog feedback
  - Very low standby current
  - Compatible with 3 V and 5 V CMOS outputs
- CurrentSense diagnostic functions
  - Multiplexed analog feedback of: load current with high precision proportional current mirror
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
  - Off-state open-load detection
  - Output short to $V_{CC}$ detection
  - Sense enable/ disable
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Loss of ground and loss of $V_{CC}$
  - Reverse battery with external components
  - Electrostatic discharge protection

## Applications

- All types of Automotive resistive, inductive and capacitive loads
- Specially intended for Automotive Signal Lamps (up to P27W or SAE1156 or LED Rear Combinations)

## Description

The VND7050AJ12-E is a double channel high-side driver manufactured using ST proprietary VIPower® technology and housed in PowerSSO-12 package. The device is designed to drive 12 V automotive grounded loads through a 3 V and 5 V CMOS compatible interface, providing protection and diagnostics.

The device integrates advanced protective functions such as load current limitation, overload active management by power limitation and overtemperature shutdown.

A current sense delivers high precision proportional load current sense in addition to the detection of overload and short circuit to ground, short to $V_{CC}$ and off-state open-load.

A sense enable pin allows off-state diagnosis to be disabled during the module low-power mode as well as external sense resistor sharing among similar devices.

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# 1 Block diagram and pin description

**Figure 1. Block diagram**

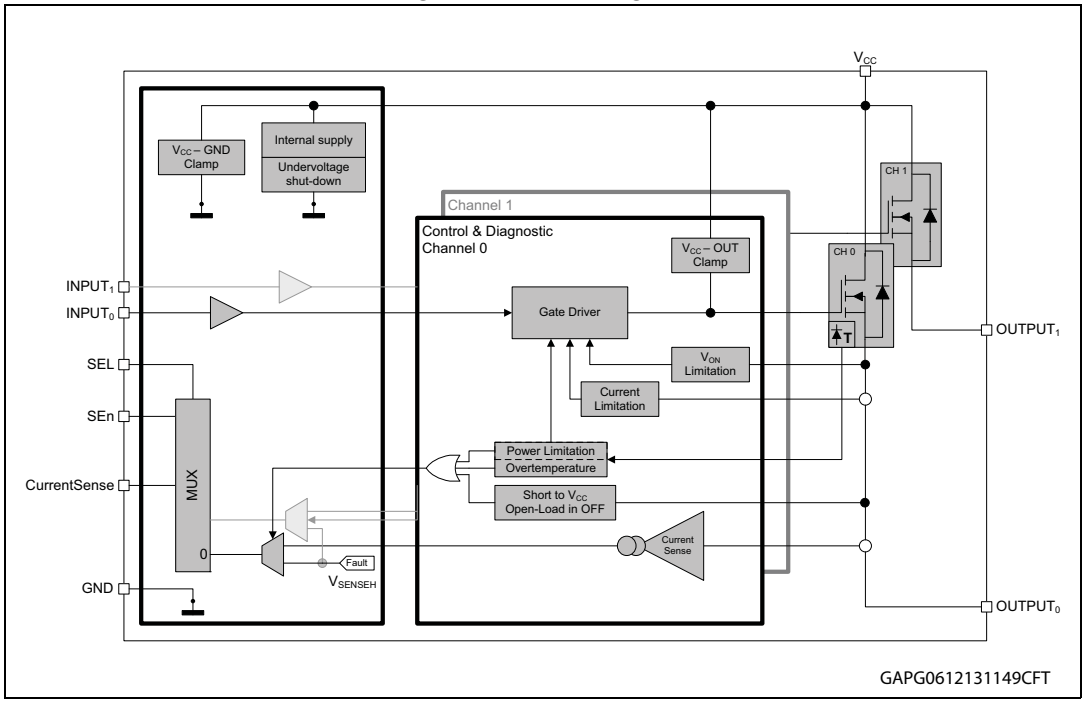



**Table 1. Pin functions**

| Name | Function |
|---|---|
| $V_{CC}$ | Battery connection. |
| $OUTPUT_{0,1}$ | Power output. |
| GND | Ground connection. Must be reverse battery protected by an external diode/resistor network. |
| $INPUT_{0,1}$ | Voltage controlled input pins with hysteresis, compatible with 3 V and 5 V CMOS outputs. They control output switch state. |
| CurrentSense | Multiplexed analog sense output pin; it delivers a current proportional to the selected diagnostic: load current, supply voltage or chip temperature. |
| SEn | Active high compatible with 3 V and 5 V CMOS outputs pin; it enables the CurrentSense diagnostic pin. |
| SEL | Active high compatible with 3 V and 5 V CMOS outputs pin; it address the CurrentSense multiplexer. |

**Figure 2. Configuration diagram (top view)**

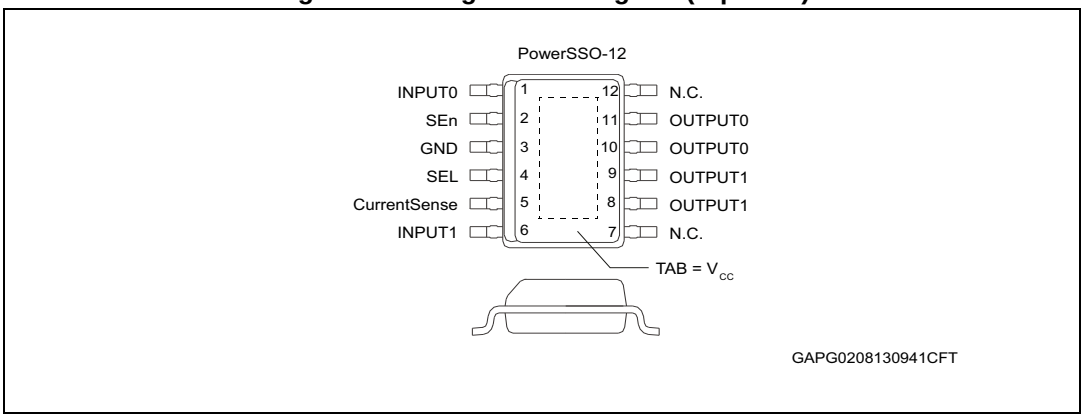


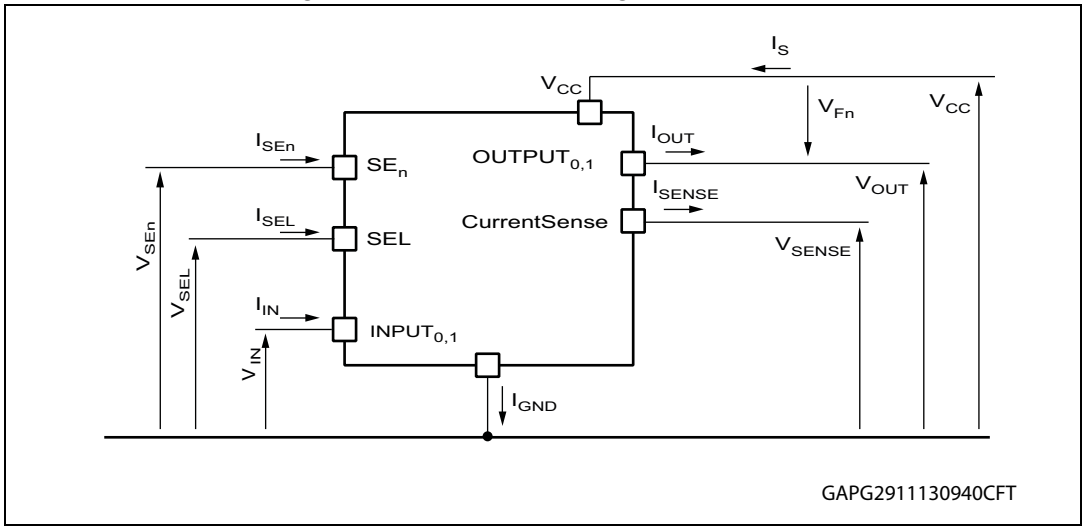

**Table 2. Suggested connections for unused and not connected pins**

| Connection/pin | CurrentSense | N.C. | Output | Input | SEn, SEL |
|---|---|---|---|---|---|
| Floating | Not allowed | X(1) | X | X | X |
| To ground | Through 1 kΩ resistor | X | Not allowed | Through 15 kΩ resistor | Through 15 kΩ resistor |

1. X: do not care.

# 2 Electrical specification

**Figure 3. Current and voltage conventions**




*Note:* *$V_{Fn} = V_{OUTn} - V_{CC}$ during reverse battery condition.*

## 2.1 Absolute maximum ratings

Stressing the device above the rating listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability.

**Table 3. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC supply voltage | 38 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 0.3 | V |
| $V_{CCPK}$ | Maximum transient supply voltage (ISO 16750-2:2010 Test B clamped to 40 V; $R_L$ = 4 Ω) | 40 | V |
| $V_{CCJS}$ | Maximum jump start voltage for single pulse short circuit protection | 28 | V |
| $-I_{GND}$ | DC reverse ground pin current | 200 | mA |
| $I_{OUT}$ | $OUTPUT_{0,1}$ DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 11 | |
| $I_{IN}$ | $INPUT_{0,1}$ DC input current | -1 to 10 | mA |
| $I_{SEn}$ | SEn DC input current | | |
| $I_{SEL}$ | SEL DC input current | | |

**Table 3. Absolute maximum ratings (continued)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{SENSE}$ | CurrentSense pin DC output current ($V_{GND}$ = $V_{CC}$ and $V_{SENSE}$ < 0 V) | 10 | mA |
| | CurrentSense pin DC output current in reverse ($V_{CC}$ < 0V) | -20 | |
| $E_{MAX}$ | Maximum switching energy (single pulse) ($T_{DEMAG}$ = 0.4 ms; $T_{jstart}$ = 150 °C) | 30 | mJ |
| $V_{ESD}$ | Electrostatic discharge (JEDEC 22A-114F)<br>– $INPUT_{0,1}$<br>– CurrentSense<br>– SEn, SEL<br>– $OUTPUT_{0,1}$<br>– $V_{CC}$ | <br>4000<br>2000<br>4000<br>4000<br>4000 | <br>V<br>V<br>V<br>V<br>V |
| $V_{ESD}$ | Charge device model (CDM-AEC-Q100-011) | 750 | V |
| $T_j$ | Junction operating temperature | -40 to 150 | °C |
| $T_{stg}$ | Storage temperature | -55 to 150 | |

## 2.2 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Typ. value | Unit |
|---|---|---|---|
| $R_{thj\text{-}board}$ | Thermal resistance junction-board (JEDEC JESD 51-5 / 51-8)(1)(2) | 6.4 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(3) | 59 | |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient (JEDEC JESD 51-7)(1)(2) | 25 | |

1. One channel ON.
2. Device mounted on four-layers 2s2p PCB.
3. Device mounted on two-layers 2s0p PCB with 2 $cm^2$ heatsink copper trace.

## 2.3 Main electrical characteristics

7 V < $V_{CC}$ < 28 V; -40 °C < $T_j$ < 150 °C, unless otherwise specified.

All typical values refer to $V_{CC}$ = 13 V; $T_j$ = 25°C, unless otherwise specified.

**Table 5. Power section**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Operating supply voltage | | 4 | 13 | 28 | V |
| $V_{USD}$ | Undervoltage shutdown | | | | 4 | |
| $V_{USDReset}$ | Undervoltage shutdown reset | | | | 5 | |
| $V_{USDhyst}$ | Undervoltage shutdown hysteresis | | | 0.3 | | |
| $R_{ON}$ | On-state resistance(1) | $I_{OUT}$ = 2 A; $T_j$ = 25 °C | | 50 | | mΩ |
| | | $I_{OUT}$ = 2 A; $T_j$ = 150 °C | | | 100 | |
| | | $I_{OUT}$ = 2 A; $V_{CC}$ = 4 V; $T_j$ = 25 °C | | | 75 | |
| $V_{clamp}$ | Clamp voltage | $I_S$ = 20 mA; $T_j$ = -40 °C | 38 | | | V |
| | | $I_S$ = 20 mA; 25°C < $T_j$ < 150°C | 41 | 46 | 52 | |
| $I_{STBY}$ | Supply current in standby at $V_{CC}$ = 13 V (2) | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{SEn}$ = 0 V; $V_{SEL}$ = 0 V; $T_j$ = 25 °C | | | 0.5 | µA |
| | | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{SEn}$ = 0 V; $V_{SEL}$ = 0 V; $T_j$ = 85 °C (3) | | | 0.5 | µA |
| | | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{SEn}$ = 0 V; $V_{SEL}$ = 0 V; $T_j$ = 125 °C | | | 3 | µA |
| $t_{D\_STBY}$ | Standby mode blanking time | $V_{CC}$ = 13 V; $V_{IN}$ = $V_{OUT}$ = $V_{SEL}$ = 0 V; $V_{SEn}$ = 5 V to 0 V | 60 | 300 | 550 | µA |
| $I_{S(ON)}$ | Supply current | $V_{CC}$ = 13 V; $V_{SEn}$ = $V_{SEL}$ = 0 V; $V_{IN0}$ = 5 V; $V_{IN1}$ = 5 V; $I_{OUT0}$ = 0 A; $I_{OUT1}$ = 0 A | | 5 | 8 | mA |
| $I_{GND(ON)}$ | Control stage current consumption in ON state. All channels active. | $V_{CC}$ = 13 V; $V_{SEn}$ = 5 V; $V_{SEL}$ = 0 V; $V_{IN0}$ = 5 V; $V_{IN1}$ = 5 V; $I_{OUT0}$ = 2 A; $I_{OUT1}$ = 2 A | | | 12 | mA |
| $I_{L(off)}$ | Off-state output current at $V_{CC}$ = 13 V(1) | $V_{IN}$ = $V_{OUT}$ = 0 V; $V_{CC}$ = 13 V; $T_j$ = 25 °C | 0 | 0.01 | 0.5 | µA |
| | | $V_{IN}$ = $V_{OUT}$ = 0 V; $V_{CC}$ = 13 V; $T_j$ = 125 °C | 0 | | 3 | |
| $V_F$ | Output - $V_{CC}$ diode voltage (1) | $I_{OUT}$ = -2 A; $T_j$ = 150 °C | | | 0.7 | V |

1. For each channel.
2. PowerMOS leakage included.
3. Parameter specified by design; not subject to production test.

**Table 6. Switching ($V_{CC}$ = 13 V; -40°C < $T_j$ < 150°C, unless otherwise specified)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ (1) | Turn-on delay time at $T_j$ = 25°C | $R_L$ = 6.5 Ω | 10 | 60 | 120 | µs |
| $t_{d(off)}$ (1) | Turn-off delay time at $T_j$ = 25°C | | 10 | 40 | 100 | |
| $(dV_{OUT}/dt)_{on}$ (1) | Turn-on voltage slope at $T_j$ = 25°C | $R_L$ = 6.5 Ω | 0.1 | 0.3 | 0.7 | V/µs |
| $(dV_{OUT}/dt)_{off}$ (1) | Turn-off voltage slope at $T_j$ = 25°C | | 0.1 | 0.32 | 0.7 | |
| $W_{ON}$ | Switching energy losses at turn-on ($t_{won}$) | $R_L$ = 6.5 Ω | — | 0.25 | 0.33 (2) | mJ |
| $W_{OFF}$ | Switching energy losses at turn-off ($t_{woff}$) | $R_L$ = 6.5 Ω | — | 0.23 | 0.31 (2) | mJ |
| $t_{SKEW}$ (1) | Differential pulse skew ($t_{PHL}$ - $t_{PLH}$) | $R_L$ = 6.5 Ω | -80 | -30 | 20 | µs |

1. See *Figure 6: Switching times and Pulse skew.*
2. Parameter guaranteed by design and characterization; not subject to production test.

**Table 7. Logic inputs (7 V < $V_{CC}$ < 28 V; -40°C < $T_j$ < 150°C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **$INPUT_{0,1}$ characteristics** | | | | | | |
| $V_{IL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{IL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $V_{IH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{IH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| $V_{I(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{ICL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |
| **SEL characteristics (7 V < $V_{CC}$ < 18 V)** | | | | | | |
| $V_{SELL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SELL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $V_{SELH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SELH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | µA |
| $V_{SEL(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SELCL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |
| **SEn characteristics (7 V < $V_{CC}$ < 18 V)** | | | | | | |
| $V_{SEnL}$ | Input low level voltage | | | | 0.9 | V |
| $I_{SEnL}$ | Low level input current | $V_{IN}$ = 0.9 V | 1 | | | µA |
| $V_{SEnH}$ | Input high level voltage | | 2.1 | | | V |
| $I_{SEnH}$ | High level input current | $V_{IN}$ = 2.1 V | | | 10 | µA |

**Table 7. Logic inputs (7 V < $V_{CC}$ < 28 V; -40°C < $T_j$ < 150°C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SEn(hyst)}$ | Input hysteresis voltage | | 0.2 | | | V |
| $V_{SEnCL}$ | Input clamp voltage | $I_{IN}$ = 1 mA | 5.3 | | 7.2 | V |
| | | $I_{IN}$ = -1 mA | | -0.7 | | |

**Table 8. Protections (7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{LIMH}$ | DC short circuit current | $V_{CC}$ = 13 V | 21 | 30 | 42 | A |
| | | 4 V < $V_{CC}$ < 18 V(1) | | | 42 | |
| $I_{LIML}$ | Short circuit current during thermal cycling | $V_{CC}$ = 13 V; $T_R < T_j < T_{TSD}$ | | 10 | | |
| $T_{TSD}$ | Shutdown temperature | | 150 | 175 | 200 | °C |
| $T_R$ | Reset temperature(1) | | $T_{RS}$ + 1 | $T_{RS}$ + 7 | | |
| $T_{RS}$ | Thermal reset of fault diagnostic indication | $V_{SEn}$ = 5 V | 135 | | | |
| $T_{HYST}$ | Thermal hysteresis ($T_{TSD}$ - $T_R$)(1) | | | 7 | | |
| $\Delta T_{J\_SD}$ | Dynamic temperature | $T_j$ = -40 °C; $V_{CC}$ = 13 V | | 60 | | K |
| $V_{DEMAG}$ | Turn-off output voltage clamp | $I_{OUT}$ = 2 A; L = 6 mH; $T_j$ = -40 °C | $V_{CC}$ - 38 | | | V |
| | | $I_{OUT}$ = 2 A; L = 6 mH; $T_j$ = 25 °C to +150 °C | $V_{CC}$ - 41 | $V_{CC}$ - 46 | $V_{CC}$ - 52 | |
| $V_{ON}$ | Output voltage drop limitation | $I_{OUT}$ = 0.2 A | | 20 | | mV |

1. Parameter guaranteed by design and characterization; not subject to production test.

**Table 9. CurrentSense (7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE\_CL}$ | CurrentSense clamp voltage | $V_{SEn}$ = 0 V; $I_{SENSE}$ = 1 mA | -17 | | -12 | V |
| | | $V_{SEn}$ = 0 V; $I_{SENSE}$ = -1 mA | | 7 | | |
| **Current Sense characteristics** | | | | | | |
| $K_{OL}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.01 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | 515 | | | |
| $dK_{cal}/K_{cal}$(1)(2) | Current sense ratio drift at calibration point | $I_{OUT}$ = 0.01 A to 0.05 A; $I_{cal}$ = 30 mA; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | -30 | | 30 | % |
| $K_{LED}$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.05 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | 630 | 1465 | 2570 | |

**Table 9. CurrentSense (7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $dK_{LED}/K_{LED}$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 0.05 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | -25 | | 25 | % |
| $K_0$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.2 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | 895 | 1365 | 2170 | |
| $dK_0/K_0$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 0.2 A; $V_{SENSE}$ = 0.5 V; $V_{SEn}$ = 5 V | -20 | | 20 | % |
| $K_1$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 0.4 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | 900 | 1315 | 1985 | |
| $dK_1/K_1$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 0.4 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | -15 | | 15 | % |
| $K_2$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 1.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | 980 | 1215 | 1470 | |
| $dK_2/K_2$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 1.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | -10 | | 10 | % |
| $K_3$ | $I_{OUT}/I_{SENSE}$ | $I_{OUT}$ = 4.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | 1095 | 1215 | 1335 | |
| $dK_3/K_3$ (1)(2) | Current sense ratio drift | $I_{OUT}$ = 4.5 A; $V_{SENSE}$ = 4 V; $V_{SEn}$ = 5 V | -5 | | 5 | % |
| $I_{SENSE0}$ | CurrentSense leakage current | CurrentSense disabled: $V_{SEn}$ = 0 V; | 0 | | 0.5 | µA |
| | | CurrentSense disabled: -1 V < $V_{SENSE}$ < 5 V (1) | -0.5 | | 0.5 | µA |
| | | CurrentSense enabled: $V_{SEn}$ = 5 V; All channel ON; $I_{OUTX}$ = 0 A; $Ch_X$ diagnostic selected; – E.g. $Ch_0$: $V_{IN0}$ = 5 V; $V_{IN1}$ = 5 V; $V_{SEL}$ = 0 V; $I_{OUT0}$ = 0 A; $I_{OUT1}$ = 2 A | 0 | | 2 | µA |
| | | CurrentSense enabled: $V_{SEn}$ = 5 V; $Ch_X$ channel OFF; $Ch_X$ diagnostic selected; – E.g. $Ch_0$: $V_{IN0}$ = 0 V; $V_{IN1}$ = 5 V; $V_{SEL}$ = 0 V; $I_{OUT1}$ = 2 A | 0 | | 2 | µA |
| $V_{OUT\_MSD}$ (1) | Output Voltage for CurrentSense shutdown | $V_{SEn}$ = 5 V; $R_{SENSE}$ = 2.7 kΩ – E.g. $Ch_0$: $V_{IN0}$ = 5 V; $V_{SEL}$ = 0 V; $I_{OUT0}$ = 2 A | | 5 | | V |

**Table 9. CurrentSense (7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{SENSE\_SAT}$ | CurrentSense saturation voltage | $V_{CC}$ = 7 V; $R_{SENSE}$ = 2.7 kΩ; $V_{SEn}$ = 5 V; $V_{IN0}$ = 5 V; $V_{SEL}$ = 0 V; $I_{OUT0}$ = 4.5 A; $T_j$ = 150°C | 5 | | | V |
| $I_{SENSE\_SAT}$(1) | CS saturation current | $V_{CC}$ = 7 V; $V_{SENSE}$ = 4 V; $V_{IN0}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL0}$ = 0 V; $V_{SEL1}$ = 0 V; $T_j$ = 150°C | 4 | | | mA |
| $I_{OUT\_SAT}$(1) | Output saturation current | $V_{CC}$ = 7 V; $V_{SENSE}$ = 4 V; $V_{IN0}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL}$ = 0 V; $T_j$ = 150°C | 6 | | | A |
| **Off-state diagnostic** | | | | | | |
| $V_{OL}$ | Off-state open-load voltage detection threshold | $V_{SEn}$ = 5 V; $Ch_X$ OFF; $Ch_X$ diagnostic selected<br>– E.g: $Ch_0$<br>$V_{IN0}$ = 0 V; $V_{SEL}$ = 0 V | 2 | 3 | 4 | V |
| $I_{L(off2)}$ | Off-state output sink current | $V_{IN}$ = 0 V; $V_{OUT}$ = $V_{OL}$ | -100 | | -15 | µA |
| $t_{DSTKON}$ | Off-state diagnostic delay time from falling edge of INPUT (see *Figure 8*) | $V_{SEn}$ = 5 V; $Ch_X$ ON to OFF transition<br>$Ch_X$ diagnostic selected<br>– E.g: $Ch_0$<br>$V_{IN0}$ = 5 V to 0 V; $V_{SEL}$ = 0 V; $I_{OUT0}$ = 0 A; $V_{OUT}$ = 4 V | 100 | 350 | 700 | µs |
| $t_{D\_OL\_V}$ | Settling time for valid OFF-state open load diagnostic indication from rising edge of SEn | $V_{IN0}$ = 0 V; $V_{IN1}$ = 0 V; $V_{SEL}$ = 0 V; $V_{OUT0}$ = 4 V; $V_{SEn}$ = 0 V to 5 V | | | 60 | µs |
| $t_{D\_VOL}$ | Off-state diagnostic delay time from rising edge of $V_{OUT}$ | $V_{SEn}$ = 5 V; $Ch_X$ OFF<br>$Ch_X$ diagnostic selected<br>– E.g: $Ch_0$<br>$V_{IN0}$ = 0 V; $V_{SEL}$ = 0 V; $V_{OUT}$ = 0 V to 4 V | | 5 | 30 | µs |
| **Fault diagnostic feedback (see *Table 10*)** | | | | | | |
| $V_{SENSEH}$ | CurrentSense output voltage in fault condition | $V_{CC}$ = 13 V; $R_{SENSE}$ = 1 kΩ<br>– E.g: $Ch_0$ in open load<br>$V_{IN0}$ = 0 V; $V_{SEn}$ = 5 V; $V_{SEL}$ = 0 V; $I_{OUT0}$ = 0 A; $V_{OUT}$ = 4 V | 5 | | 6.6 | V |

**Table 9. CurrentSense (7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C) (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SENSEH}$ | CurrentSense output current in fault condition | $V_{CC}$ = 13 V; $V_{SENSE}$ = 5 V | 7 | 20 | 30 | mA |
| **CurrentSense timings (current sense mode - see *Figure 7*)** | | | | | | |
| $t_{DSENSE1H}$ | Current sense settling time from rising edge of SEn | $V_{IN}$ = 5 V; $V_{SEn}$ = 0 V to 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | | 60 | µs |
| $t_{DSENSE1L}$ | Current sense disable delay time from falling edge of SEn | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V to 0 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | 5 | 20 | µs |
| $t_{DSENSE2H}$ | Current sense settling time from rising edge of INPUT | $V_{IN}$ = 0 V to 5 V; $V_{SEn}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | 100 | 250 | µs |
| $\Delta t_{DSENSE2H}$ | Current sense settling time from rising edge of $I_{OUT}$ (dynamic response to a step change of $I_{OUT}$) | $V_{IN}$ = 5 V; $V_{SEn}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $I_{SENSE}$ = 90 % of $I_{SENSEMAX}$; $R_L$ = 6.5 Ω | | | 100 | µs |
| $t_{DSENSE2L}$ | Current sense turn-off delay time from falling edge of INPUT | $V_{IN}$ = 5 V to 0 V; $V_{SEn}$ = 5 V; $R_{SENSE}$ = 1 kΩ; $R_L$ = 6.5 Ω | | 50 | 250 | µs |
| **CurrentSense timings (Multiplexer transition times)(3)** | | | | | | |
| $t_{D\_XtoY}$ | CurrentSense transition delay from $Ch_X$ to $Ch_Y$ | $V_{IN0}$ = 5 V; $V_{IN1}$ = 5 V; $V_{SEn}$ = 5 V; $V_{SEL}$ = 0 V to 5 V; $I_{OUT0}$ = 0A; $I_{OUT1}$ = 3 A; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |
| $t_{D\_CStoVSENSEH}$ | CurrentSense transition delay from stable current sense on $Ch_X$ to $V_{SENSEH}$ on $Ch_Y$ | $V_{IN0}$ = 5 V; $V_{IN1}$ = 0 V; $V_{SEn}$ = 5 V; $V_{SEL}$ = 0 V to 5 V; $I_{OUT0}$ = 3 A; $V_{OUT1}$ = 4 V; $R_{SENSE}$ = 1 kΩ | | | 20 | µs |

1. Parameter guaranteed by design and characterization; not subject to production test.
2. All values refer to $V_{CC}$ = 13 V; $T_j$ = 25°C, unless otherwise specified.
3. Transition delay are measured up to +/- 10% of final conditions.

Figure 4. $I_{OUT}/I_{SENSE}$ versus $I_{OUT}$

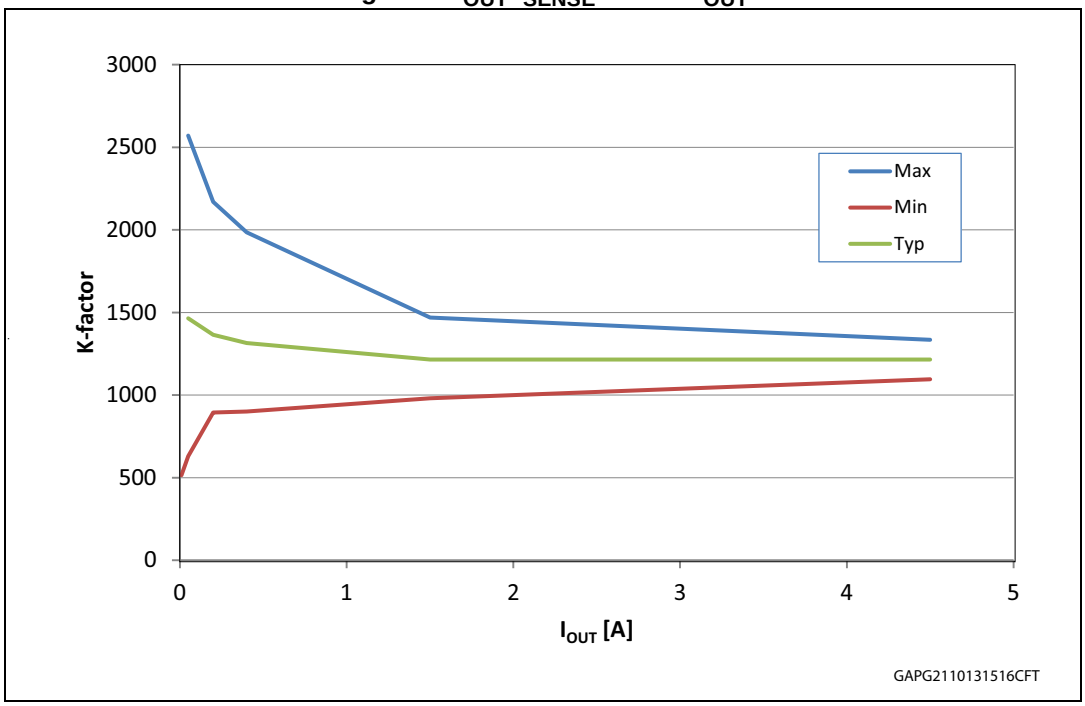



Figure 5. Current sense accuracy versus $I_{OUT}$

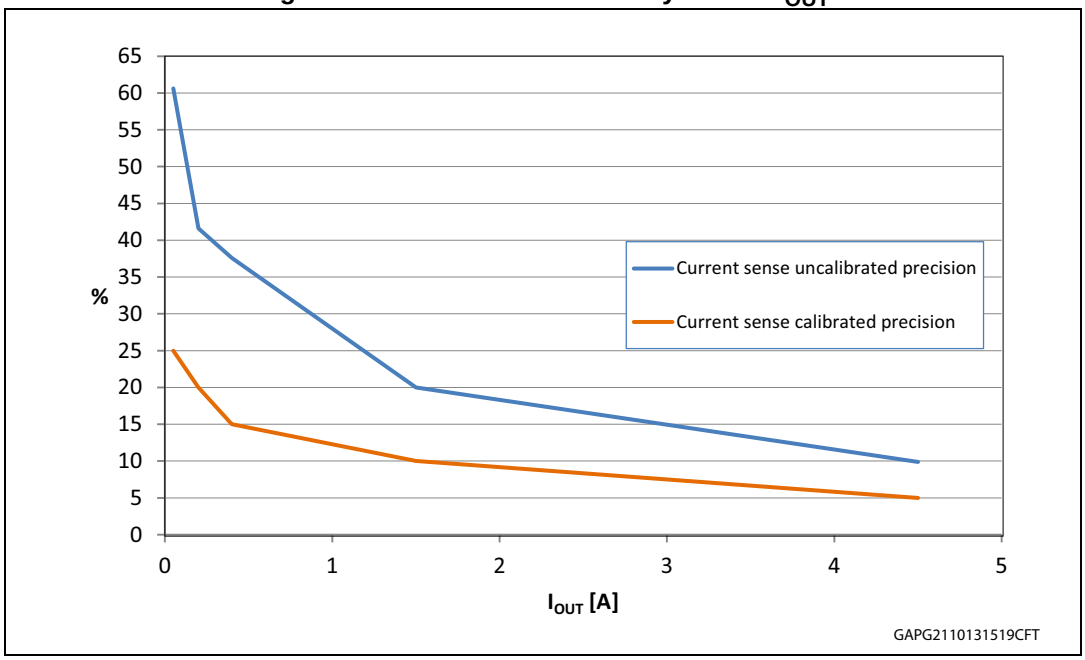


**Figure 6. Switching times and Pulse skew**

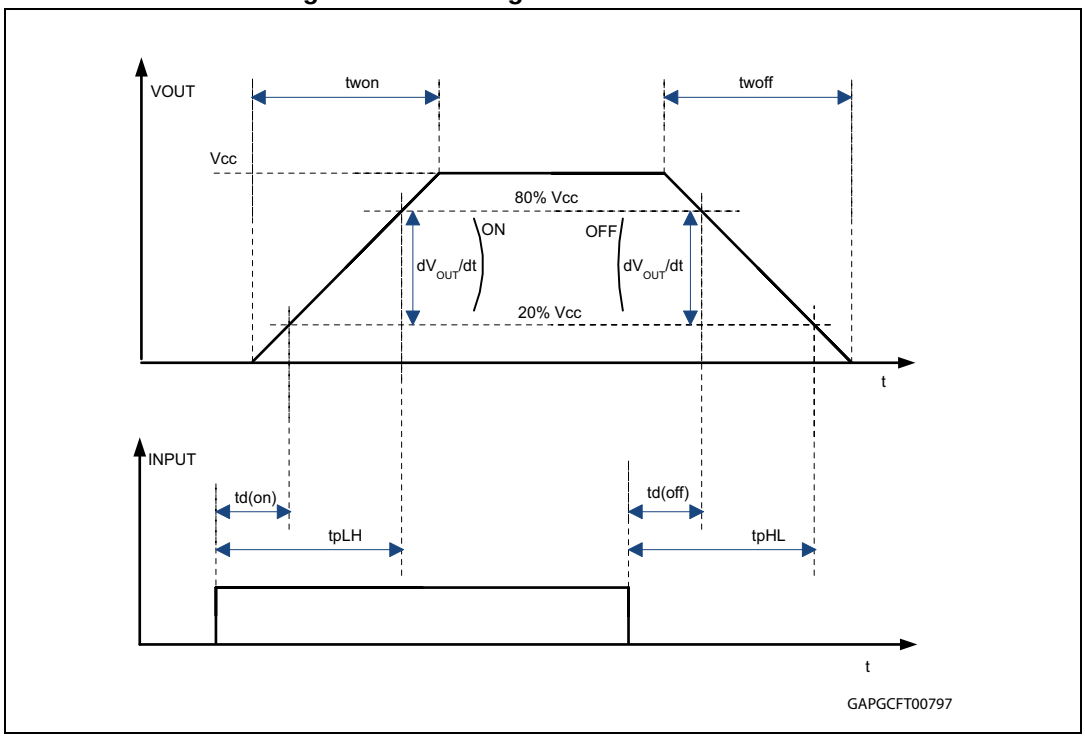



**Figure 7. CurrentSense timings**

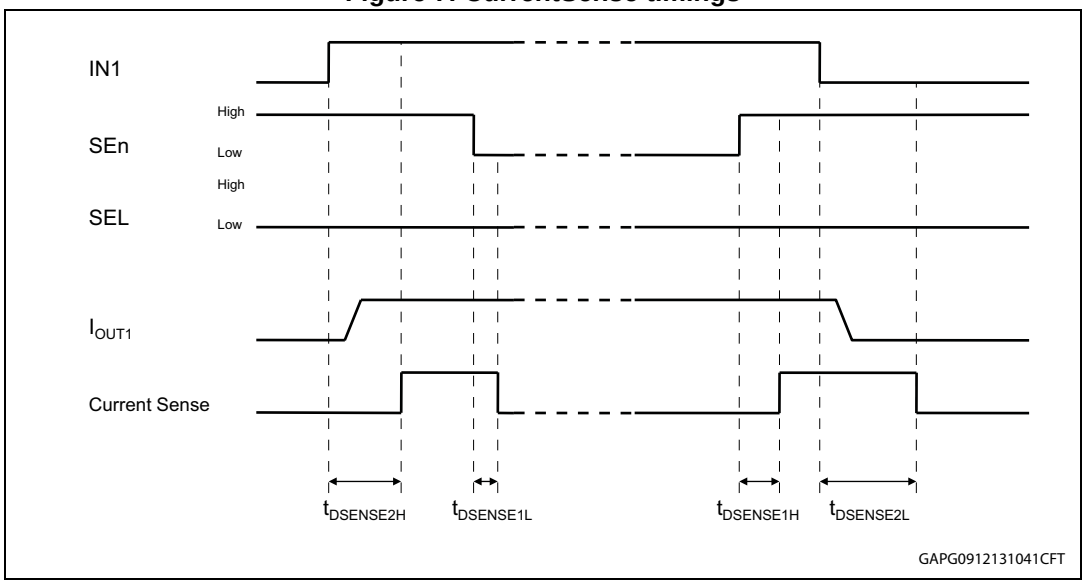


Figure 8. $T_{DSTKON}$

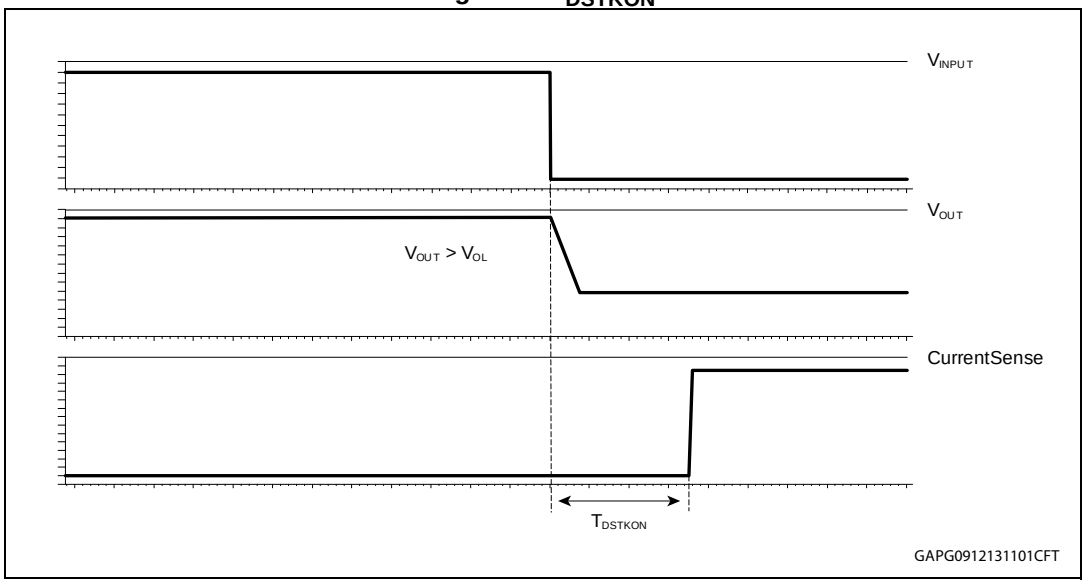



Table 10. Truth table

| Mode | Conditions | $IN_X$ | SEn | SEL | $OUT_X$ | CurrentSense | Comments |
|---|---|---|---|---|---|---|---|
| Standby | All logic inputs low | L | L | L | L | Hi-Z | Low quiescent current consumption |
| Normal | Nominal load connected; $T_j$ < 150°C | L | Refer to *Table 11* | | L | Refer to *Table 11* | |
| | | H | | | H | | Outputs configured for auto-restart |
| | | H | | | H | | Outputs configured for latch off |
| Overload | Overload or short to GND causing: $T_j > T_{TSD}$ or $\Delta T_j > \Delta T_{j\_SD}$ | L | Refer to *Table 11* | | L | Refer to *Table 11* | |
| | | H | | | H | | Output cycles with temperature hysteresis |
| | | H | | | L | | Output latches off |
| Under-voltage | $V_{CC} < V_{USD}$ (falling) | X | X | X | L<br>L | Hi-Z<br>Hi-Z | Re-start when $V_{CC} > V_{USD} + V_{USDhyst}$ (rising) |
| Off-state diagnostics | Short to $V_{CC}$ | L | Refer to *Table 11* | | H | Refer to *Table 11* | |
| | Open-load | L | | | H | | External pull up |
| Negative output voltage | Inductive loads turn-off | L | Refer to *Table 11* | | < 0 V | Refer to *Table 11* | |

**Table 11. CurrentSense multiplexer addressing**

| SEn | SEL | MUX channel | CurrentSense output | | | |
|---|---|---|---|---|---|---|
| | | | Normal mode | Overload | Off-state diag. | Negative output |
| L | X | | Hi-Z | | | |
| H | L | Channel 0 diagnostic | $I_{SENSE}$ = 1/K * $I_{OUT0}$ | $V_{SENSE}$ = $V_{SENSEH}$ | $V_{SENSE}$ = $V_{SENSEH}$ | Hi-Z |
| H | H | Channel 1 diagnostic | $I_{SENSE}$ = 1/K * $I_{OUT1}$ | $V_{SENSE}$ = $V_{SENSEH}$ | $V_{SENSE}$ = $V_{SENSEH}$ | Hi-Z |

## 2.4 Waveforms

**Figure 9. Standby mode activation**

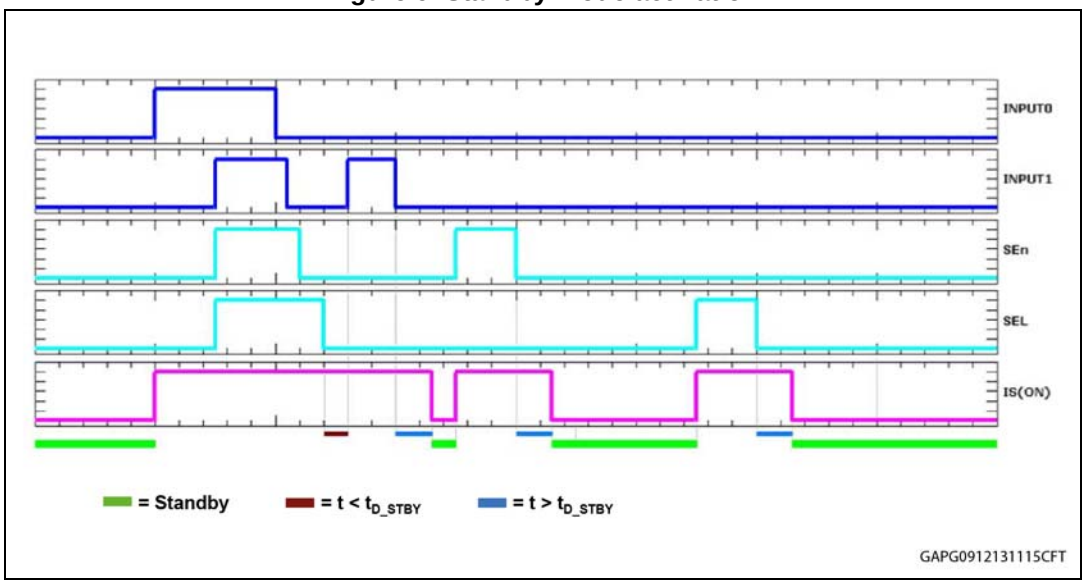
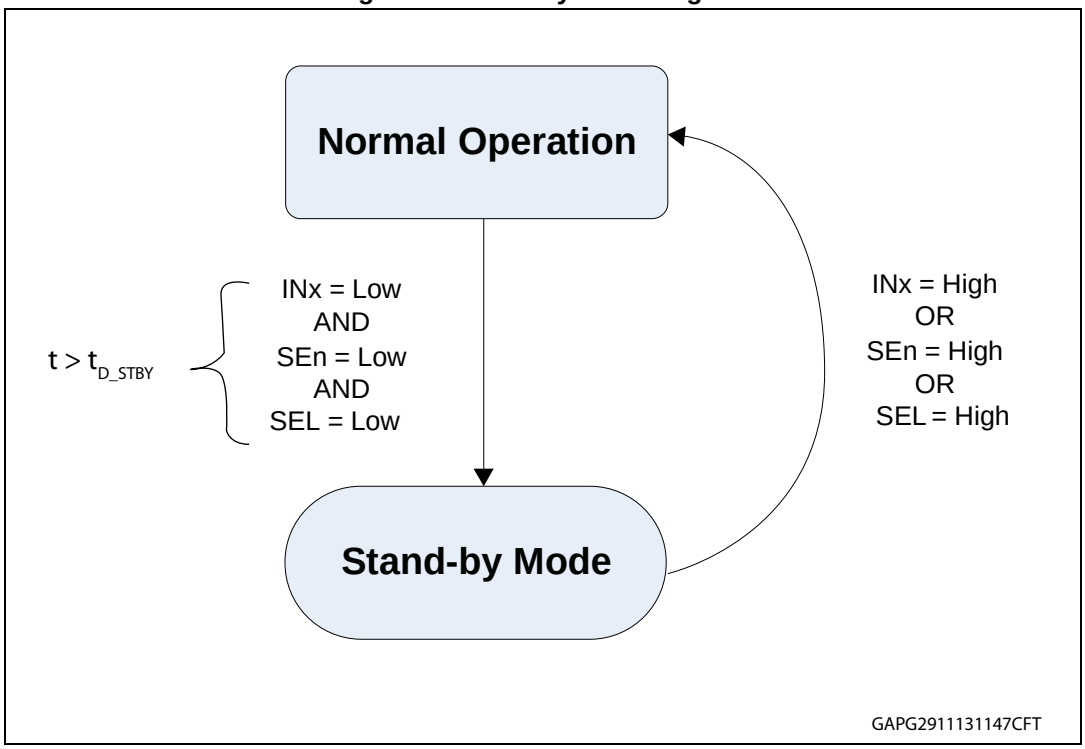


**Figure 10. Standby state diagram**



## 2.5 Electrical characteristics curves

**Figure 11. OFF-state output current**

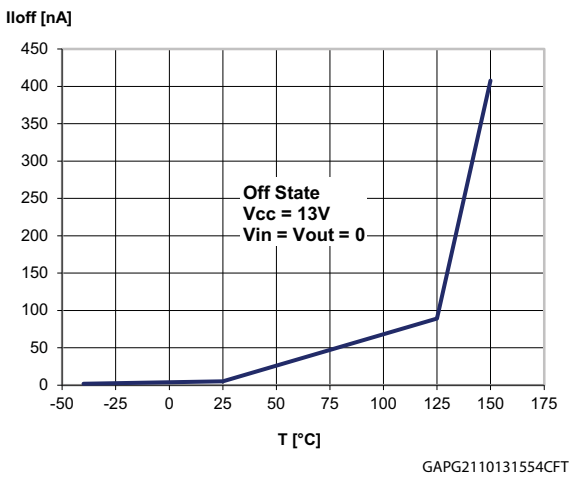



**Figure 12. Standby current**

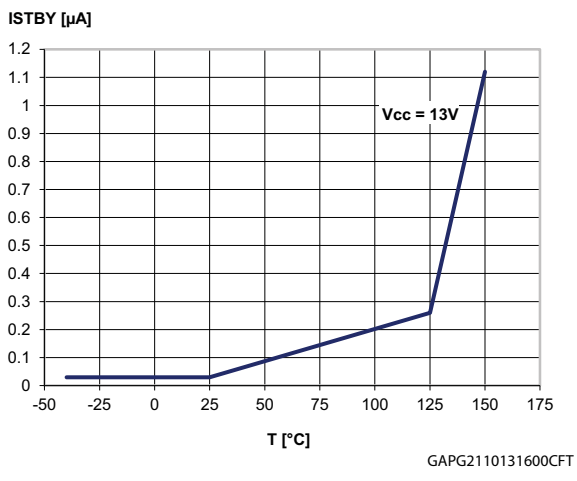



**Figure 13. $I_{GND(ON)}$ vs. $I_{out}$**

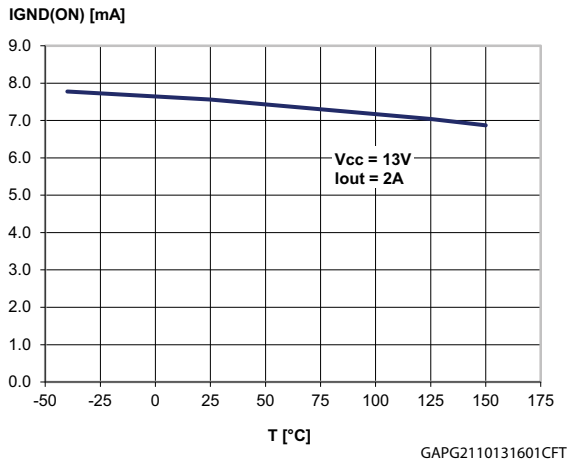



**Figure 14. Logic Input high level voltage**

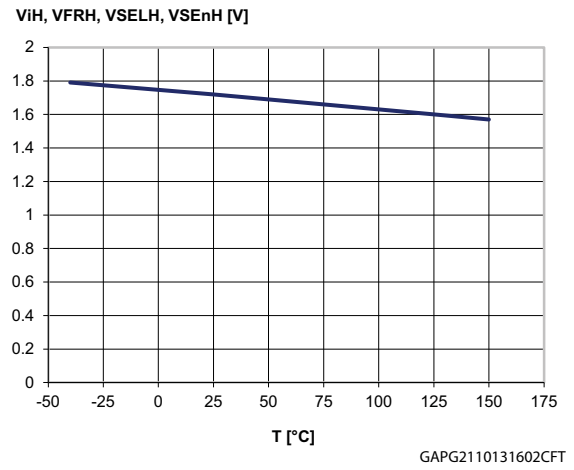



**Figure 15. Logic Input low level voltage**

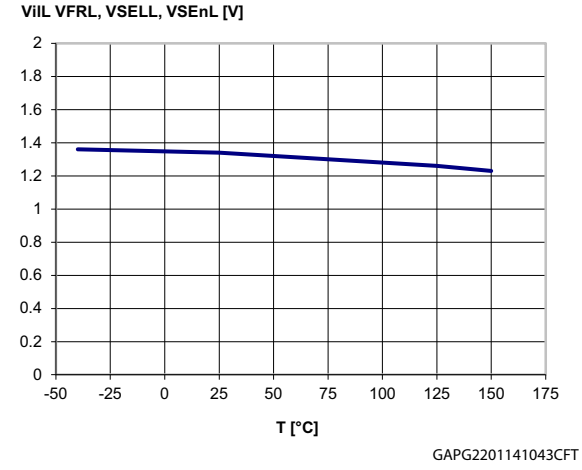



**Figure 16. High level logic input current**

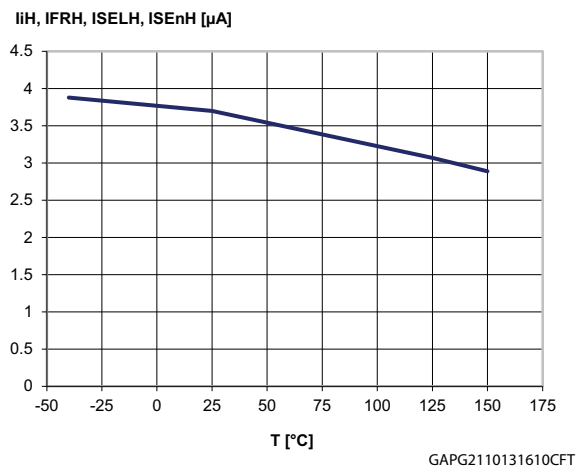


**Figure 17. Low level logic input current**

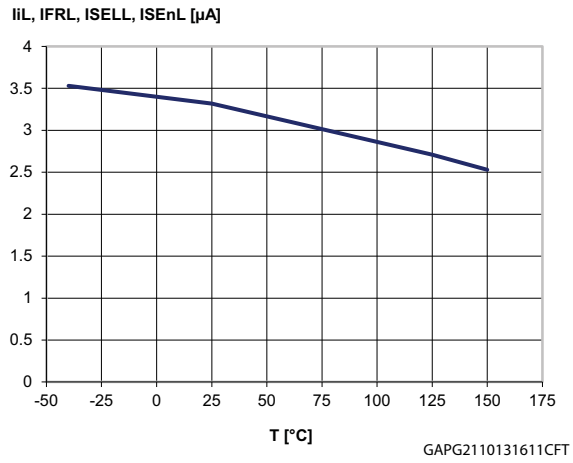



**Figure 18. Logic Input hysteresis voltage**

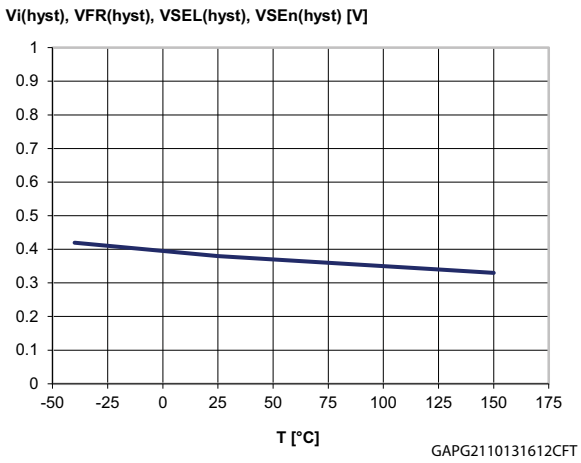



**Figure 19. Undervoltage shutdown**

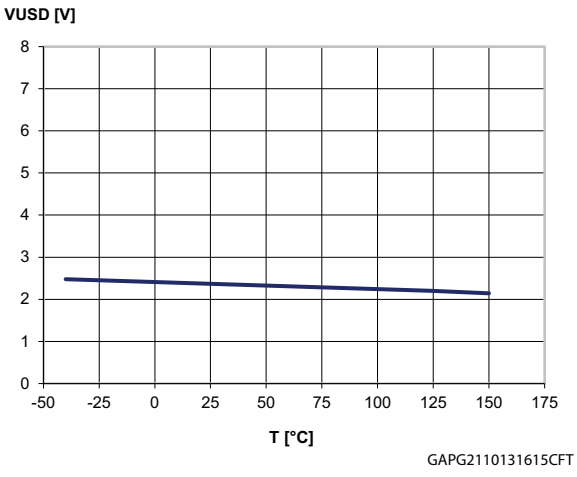



**Figure 20. On-state resistance vs. $T_{case}$**

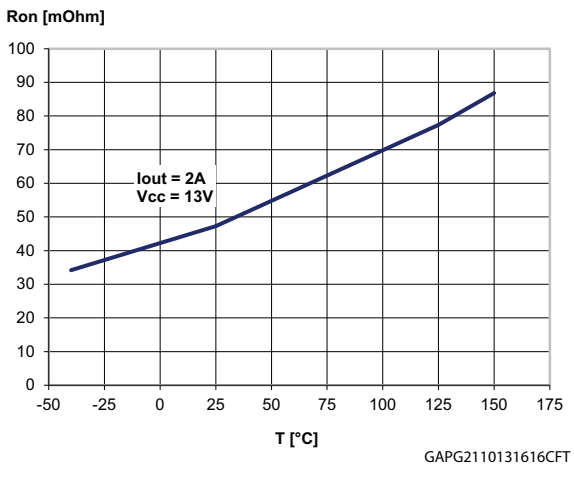



**Figure 21. On-state resistance vs. $V_{CC}$**

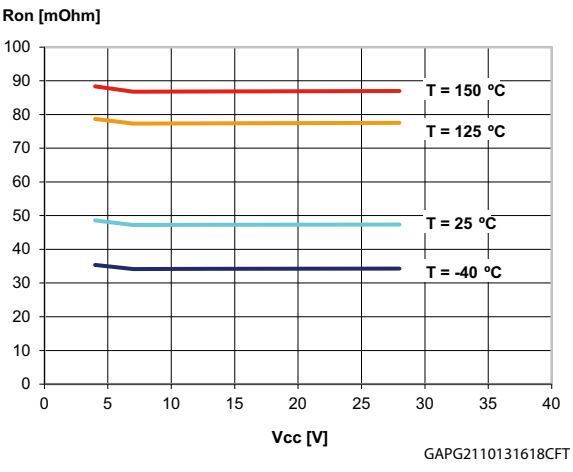



**Figure 22. Turn-on voltage slope**

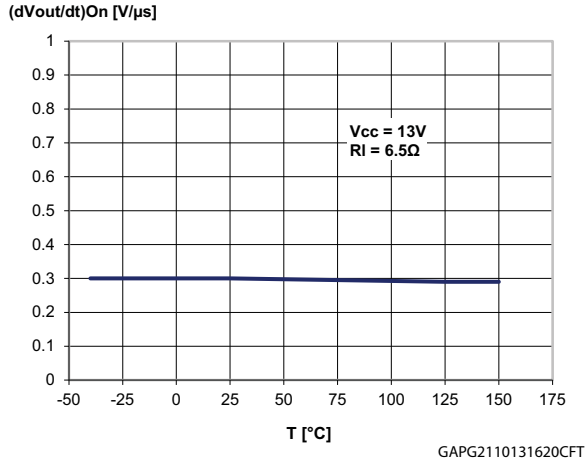


**Figure 23. Turn-off voltage slope**

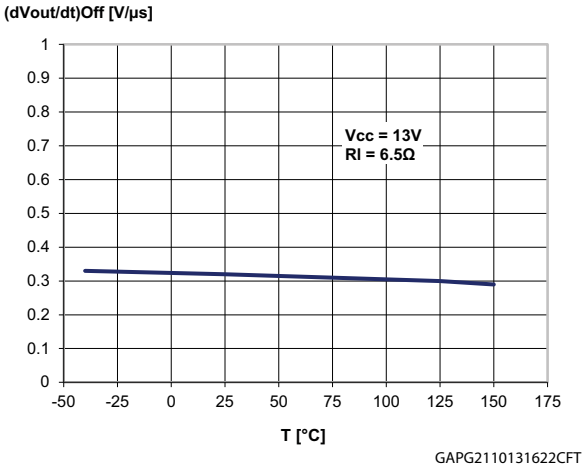



**Figure 24. $W_{on}$ vs $T_{case}$**

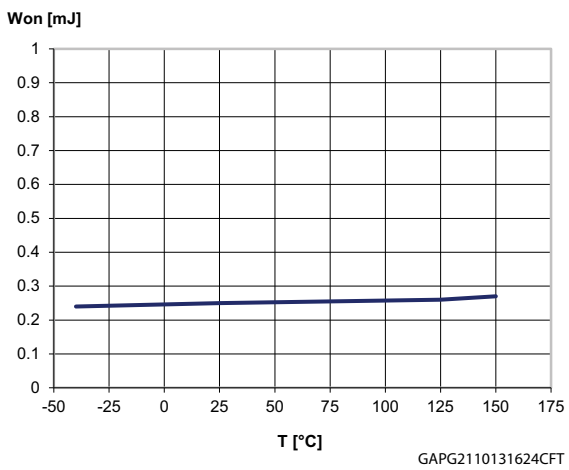



**Figure 25. $W_{off}$ vs $T_{case}$**

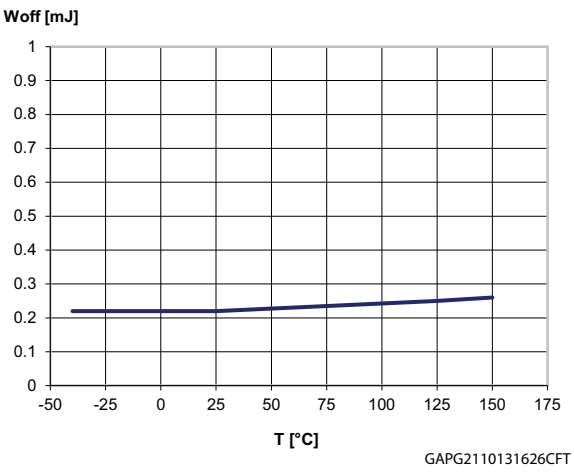



**Figure 26. $I_{LIMH}$ vs. $T_{case}$**

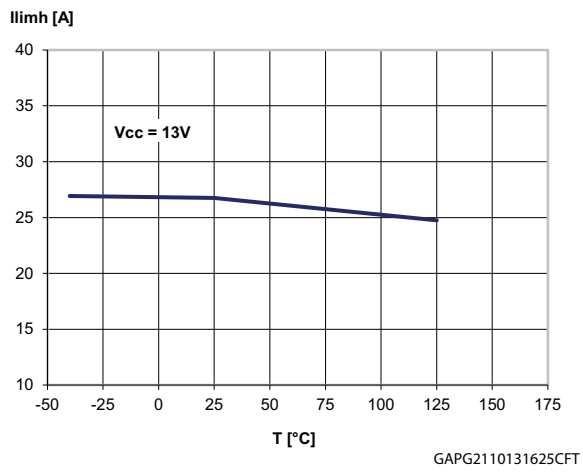



**Figure 27. OFF-state open-load voltage detection threshold**

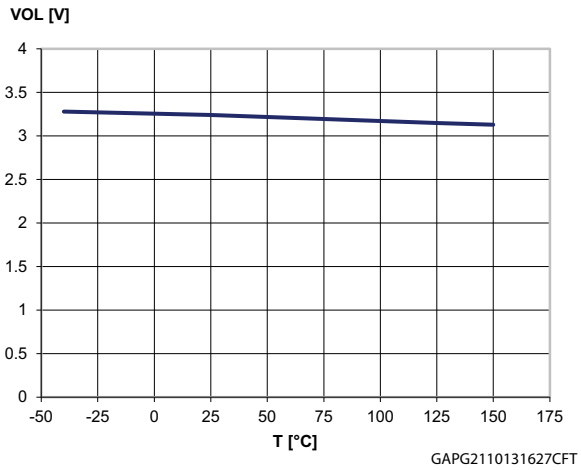



**Figure 28. $V_{sense}$ clamp vs $T_{case}$**

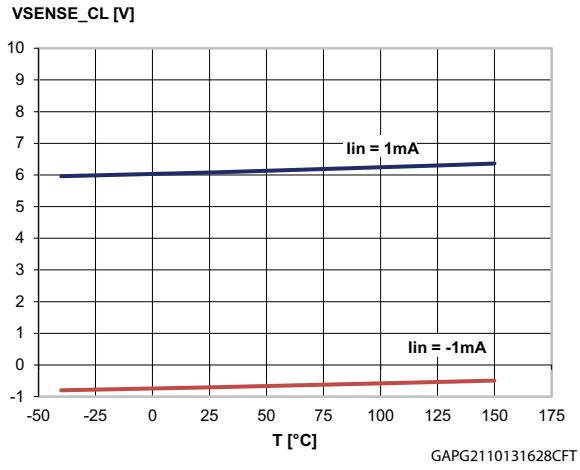
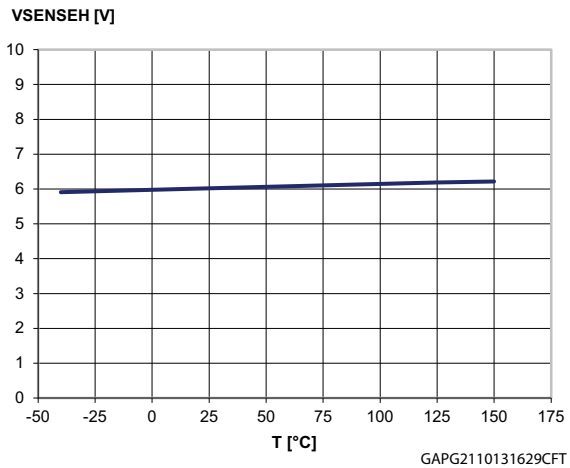


**Figure 29. $V_{senseh}$ vs $T_{case}$**



# 3 Protections

## 3.1 Power limitation

The basic working principle of this protection consists of an indirect measurement of the junction temperature swing $\Delta T_j$ through the direct measurement of the spatial temperature gradient on the device surface in order to automatically shut off the output MOSFET as soon as $\Delta T_j$ exceeds the safety level of $\Delta T_{j\_SD}$. The output MOSFET switches on and cycles with a thermal hysteresis according to the maximum instantaneous power which can be handled. The protection prevents fast thermal transient effects and, consequently, reduces thermo-mechanical fatigue.

## 3.2 Thermal shutdown

In case the junction temperature of the device exceeds the maximum allowed threshold (typically 175°C), it automatically switches off and the diagnostic indication is triggered. The device switches on again as soon as its junction temperature drops to $T_R$.

## 3.3 Current limitation

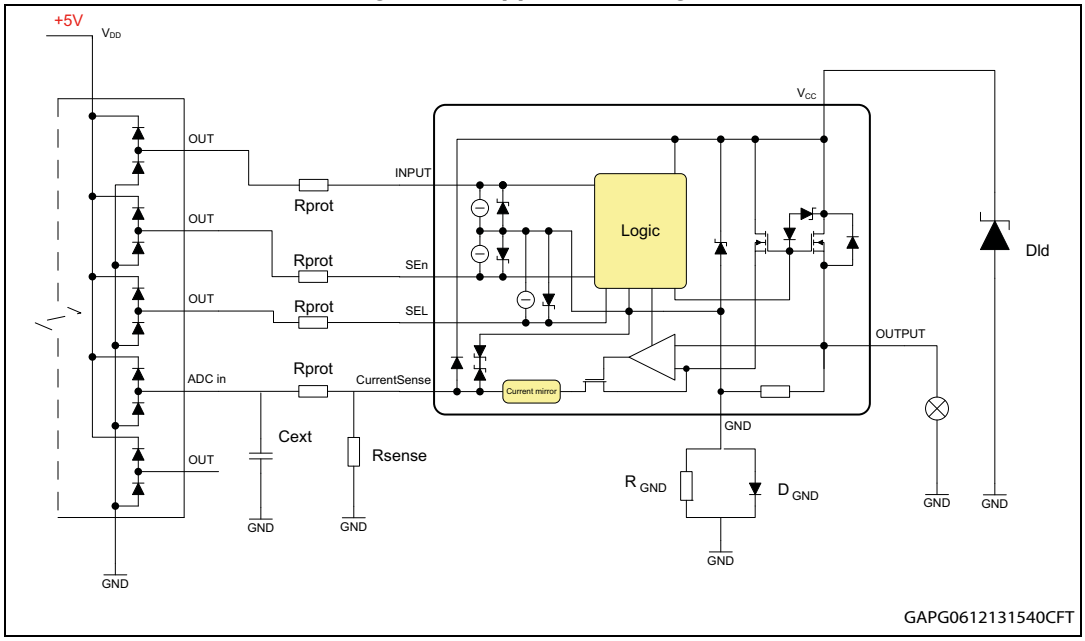
The device is equipped with an output current limiter in order to protect the silicon as well as the other components of the system (e.g. bonding wires, wiring harness, connectors, loads, etc.) from an excessive current flow. Consequently, in case of short circuit, overload or during load power-up, the output current is clamped to a safety level, $I_{LIMH}$, by operating the output power MOSFET in the active region.

## 3.4 Negative voltage clamp

In case the device drives inductive load, the output voltage reaches negative value during turn off. A negative voltage clamp structure limits the maximum negative voltage to a certain value, $V_{DEMAG}$ (see *Table 8*), allowing the inductor energy to be dissipated without damaging the device.

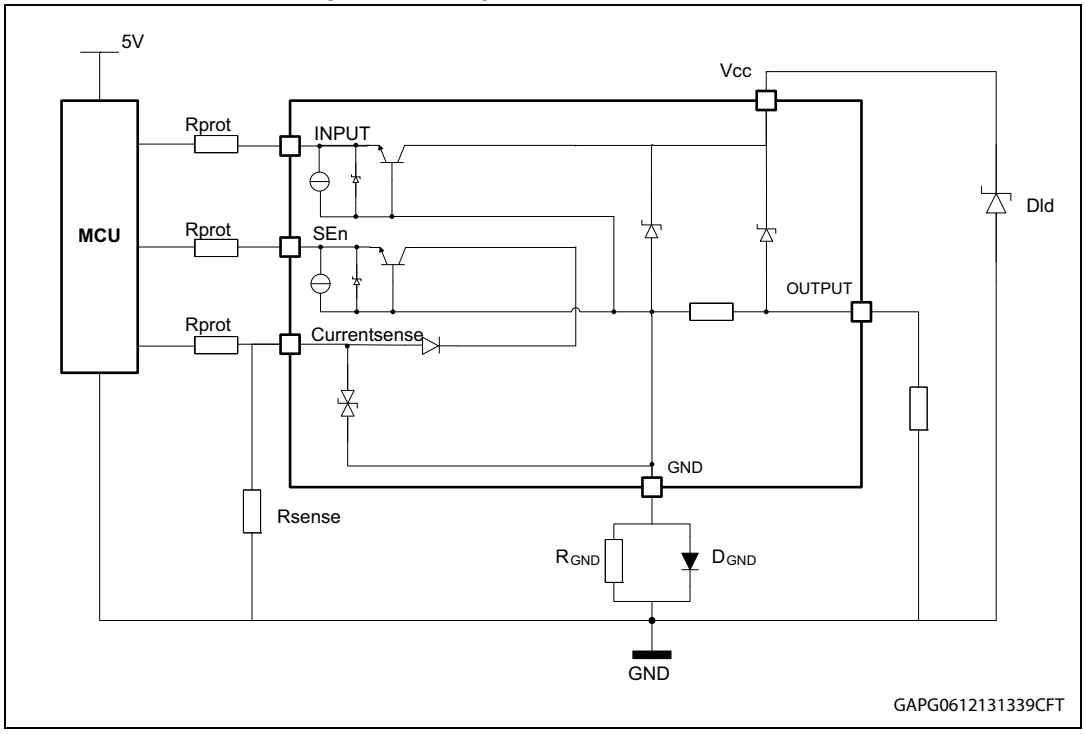
# 4 Application information

**Figure 30. Application diagram**




## 4.1 GND protection network against reverse battery

**Figure 31. Simplified internal structure**



### 4.1.1 Diode ($D_{GND}$) in the ground line

A resistor (typ. $R_{GND}$ = 4.7 kΩ) should be inserted in parallel to $D_{GND}$ if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network produces a shift (≈600 mV) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift does not vary if more than one HSD shares the same diode/resistor network.

## 4.2 Immunity against transient electrical disturbances

The immunity of the device against transient electrical emissions, conducted along the supply lines and injected into the $V_{CC}$ pin, is tested in accordance with ISO7637-2:2011 (E) and ISO 16750-2:2010.

The related function performance status classification is shown in *Table 12*.

Test pulses are applied directly to DUT (Device Under Test) both in ON and OFF-state and in accordance to ISO 7637-2:2011(E), chapter 4. The DUT is intended as the present device only, without components and accessed through $V_{CC}$ and GND terminals.

Status II is defined in ISO 7637-1 Function Performance Status Classification (FPSC) as follows: “The function does not perform as designed during the test but returns automatically to normal operation after the test”.

**Table 12. ISO 7637-2 - electrical transient conduction along supply line**

| Test Pulse 2011(E) | Test pulse severity level with Status II functional performance status | | Minimum number of pulses or test time | Burst cycle / pulse repetition time | | Pulse duration and pulse generator internal impedance |
|---|---|---|---|---|---|---|
| | Level | $U_S$(1) | | min | max | |
| 1 | III | -112V | 500 pulses | 0,5 s | | 2ms, 10Ω |
| 2a | III | +55V | 500 pulses | 0,2 s | 5 s | 50µs, 2Ω |
| 3a | IV | -220V | 1h | 90 ms | 100 ms | 0.1µs, 50Ω |
| 3b | IV | +150V | 1h | 90 ms | 100 ms | 0.1µs, 50Ω |
| 4(2) | IV | -7V | 1 pulse | | | 100ms, 0.01Ω |
| **Load dump according to ISO 16750-2:2010** | | | | | | |
| Test B(3) | | 40V | 5 pulse | 1 min | | 400ms, 2Ω |

1. $U_S$ is the peak amplitude as defined for each test pulse in ISO 7637-2:2011(E), chapter 5.6.
2. Test pulse from ISO 7637-2:2004(E).
3. With 40 V external suppressor referred to ground (-40°C < $T_j$ < 150°C).

## 4.3 MCU I/Os protection

If a ground protection network is used and negative transients are present on the $V_{CC}$ line, the control pins will be pulled negative. ST suggests to insert a resistor ($R_{prot}$) in line both to prevent the microcontroller I/O pins from latching-up and to protect the HSD inputs.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of microcontroller I/Os.

**Equation 1**

$V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For $V_{CCpeak}$ = -150 V; $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

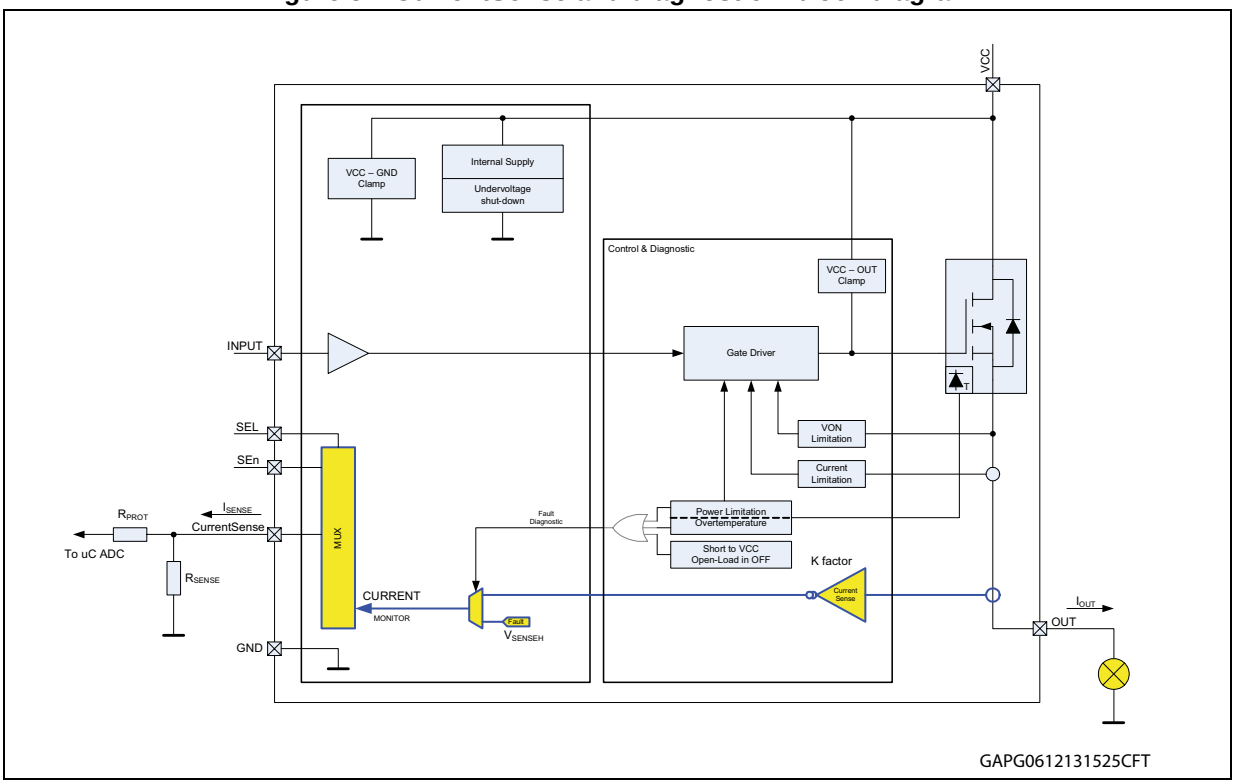
$$7.5\ k\Omega \leq R_{prot} \leq 140\ k\Omega.$$

Recommended values: $R_{prot}$ = 15 kΩ

## 4.4 CurrentSense - analog current sense

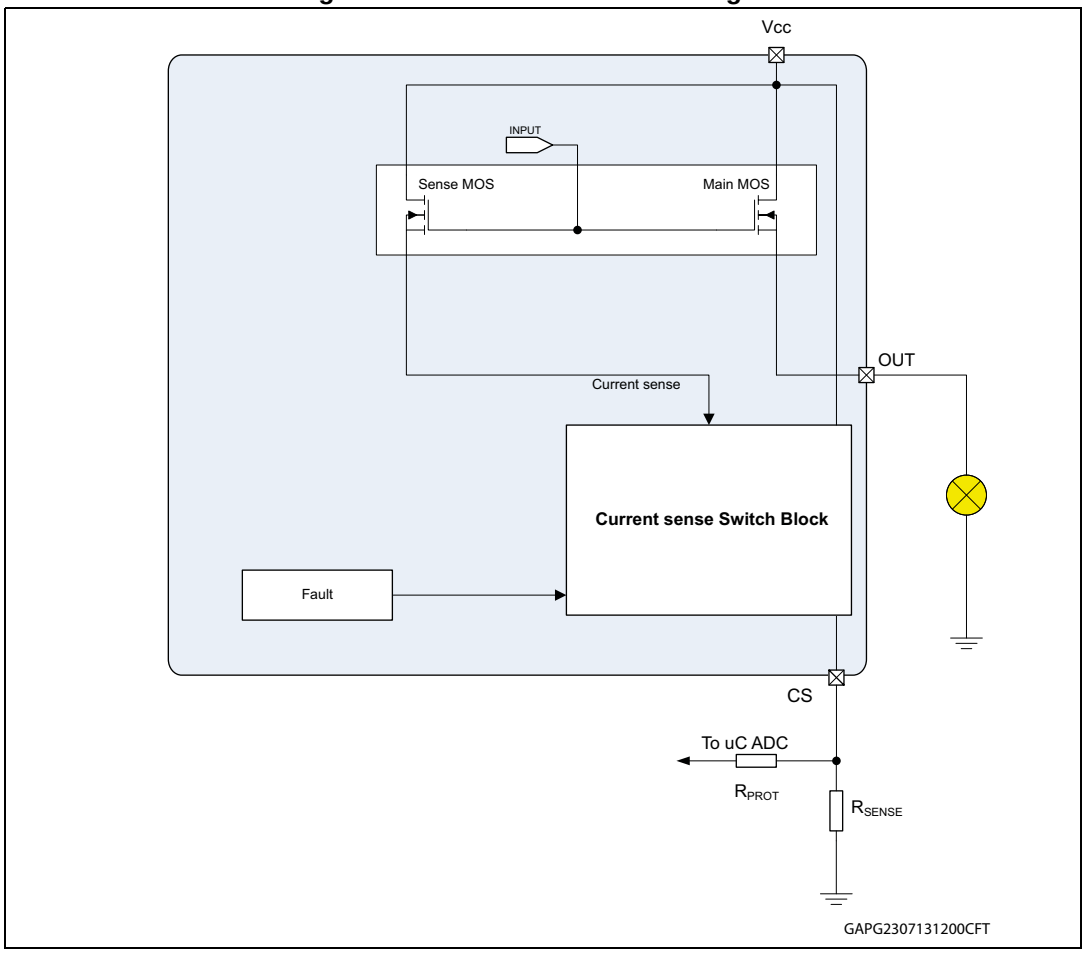
Diagnostic information on device and load status are provided by an analog output pin (CurrentSense) delivering a current mirror of channel output current

**Figure 32. CurrentSense and diagnostic – block diagram**



### 4.4.1 Principle of CurrenSense signal generation

**Figure 33. CurrentSense block diagram**




#### Current monitor

This output is capable of providing:

- **Current mirror proportional to the load current in normal operation**, delivering current proportional to the load according to known ratio named **K**
- **Diagnostics flag in fault conditions** delivering fixed voltage $V_{SENSEH}$

The current delivered by the current sense circuit, $I_{SENSE}$, can be easily converted to a voltage $V_{SENSE}$ by using an external sense resistor, $R_{SENSE}$, allowing continuous load monitoring and abnormal condition detection.

#### Normal operation (channel ON, no fault, SEn active)

While device is operating in normal conditions (no fault intervention), $V_{SENSE}$ calculation can be done using simple equations

Current provided by CurrentSense output: $I_{SENSE} = I_{OUT}/K$

Voltage on $R_{SENSE}$: $V_{SENSE} = R_{SENSE} \cdot I_{SENSE} = R_{SENSE} \cdot I_{OUT}/K$

Where :

- $V_{SENSE}$ is voltage measurable on $R_{SENSE}$ resistor
- $I_{SENSE}$ is current provided from CurrentSense pin in current output mode
- $I_{OUT}$ is current flowing through output
- K factor represents the ratio between PowerMOS cells and SenseMOS cells; its spread includes geometric factor spread, current sense amplifier offset and process parameters spread of overall circuitry specifying ratio between $I_{OUT}$ and $I_{SENSE}$.

### Failure flag indication

In case of power limitation/overtemperature, the fault is indicated by the CurrentSense pin which is switched to a “current limited” voltage source, $V_{SENSEH}$ (see *Table 9*).

In any case, the current sourced by the CurrentSense in this condition is limited to $I_{SENSEH}$ (see *Table 9*).

The typical behavior in case of overload or hard short circuit is shown in *Figure 9*.

**Figure 34. Analogue HSD – open-load detection in off-state**

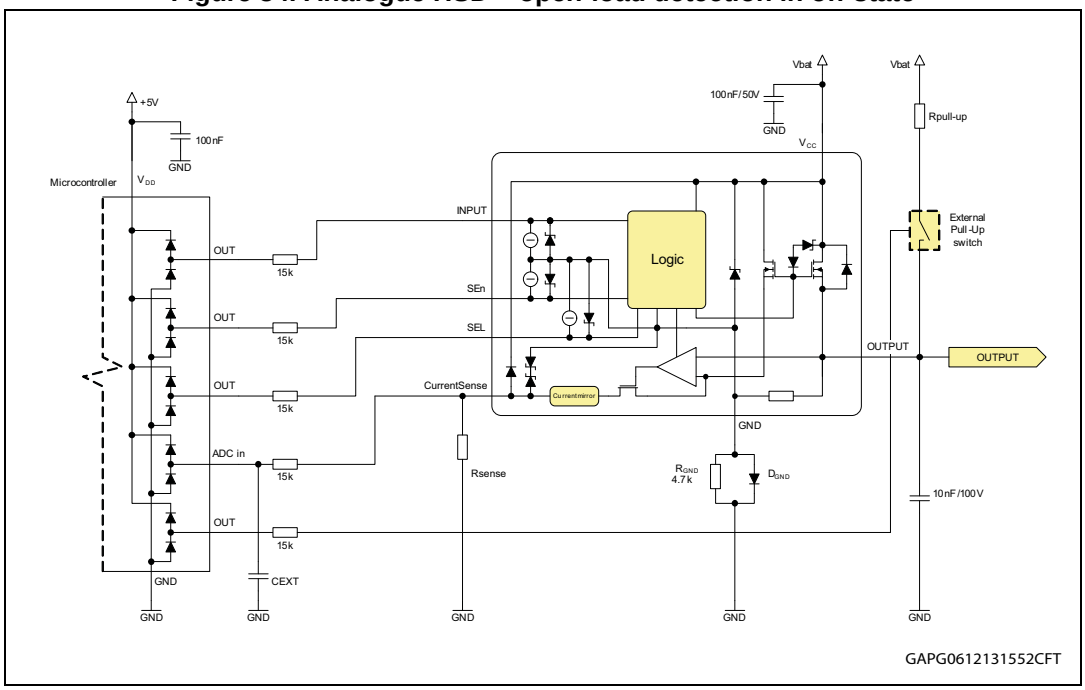


**Figure 35. Open-load / short to $V_{CC}$ condition**

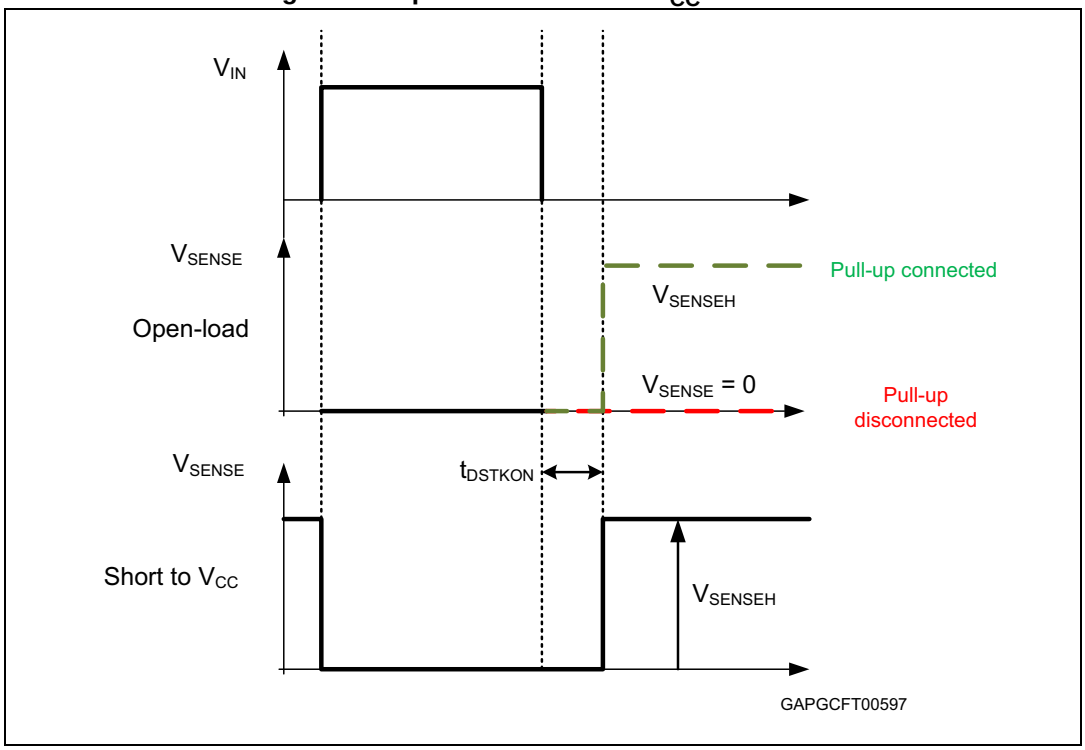



**Table 13. CurrentSense pin levels in off-state**

| Condition | Output | CurrentSense | SEn |
|---|---|---|---|
| Open-load | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | $V_{SENSEH}$ | H |
| | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |
| Short to $V_{CC}$ | $V_{OUT} > V_{OL}$ | Hi-Z | L |
| | | $V_{SENSEH}$ | H |
| Nominal | $V_{OUT} < V_{OL}$ | Hi-Z | L |
| | | 0 | H |

### 4.4.2 Short to $V_{CC}$ and OFF-state open-load detection

Short to $V_{CC}$

A short circuit between $V_{CC}$ and output is indicated by the relevant current sense pin set to $V_{SENSEH}$ during the device off-state. Small or no current is delivered by the current sense during the on-state depending on the nature of the short circuit.

OFF-state open-load with external circuitry

Detection of an open-load in off mode requires an external pull-up resistor $R_{PU}$ connecting the output to a positive supply voltage $V_{PU}$.

It is preferable $V_{PU}$ to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

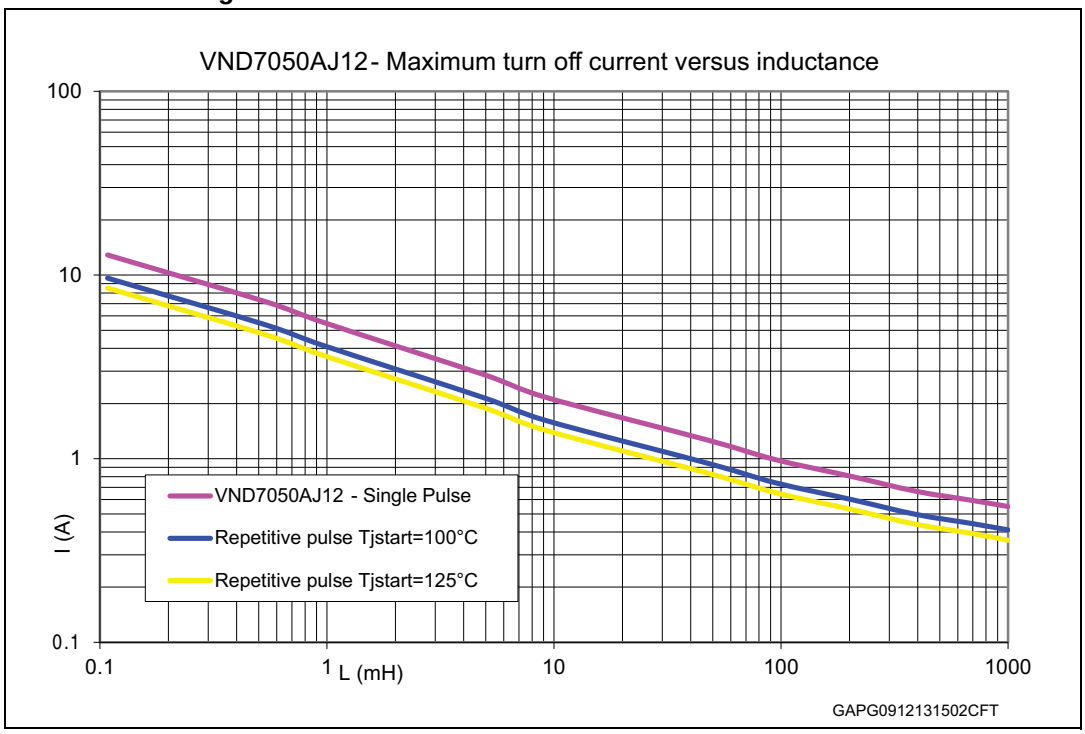
$R_{PU}$ must be selected in order to ensure $V_{OUT} > V_{OLmax}$ in accordance with the following equation:

**Equation 2**

$$R_{PU} < \frac{V_{PU} - 4}{I_{L(off2)min\ @\ 4V}}$$

## 4.5 Maximum demagnetization energy ($V_{CC}$ = 16 V)

**Figure 36. Maximum turn off current versus inductance**




1. Values are generated with $R_L$ = 0 Ω.
In case of repetitive pulses, $T_{jstart}$ (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

# 5 Package and PCB thermal data

## 5.1 PowerSSO-12 thermal data

**Figure 37. PowerSSO-12 on two-layers PCB (2s0p to JEDEC JESD 51-5)**

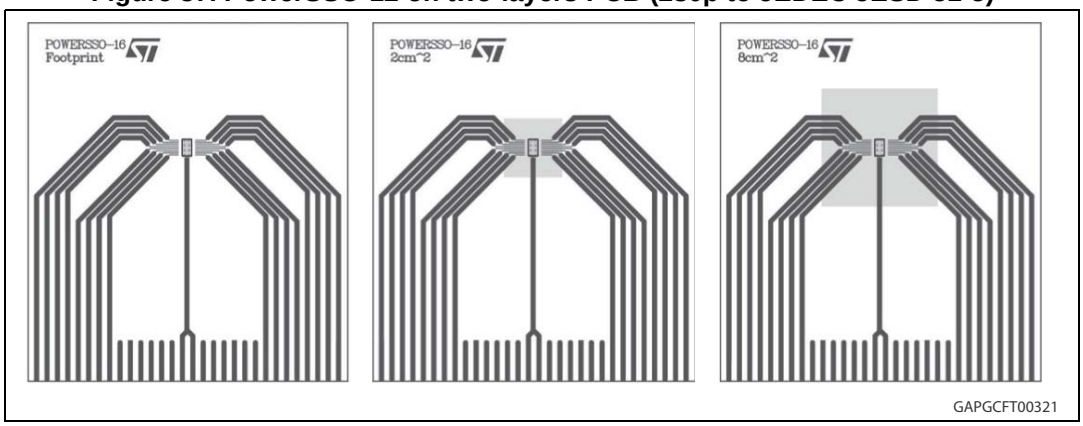



**Figure 38. PowerSSO-12 on four-layers PCB (2s2p to JEDEC JESD 51-7)**

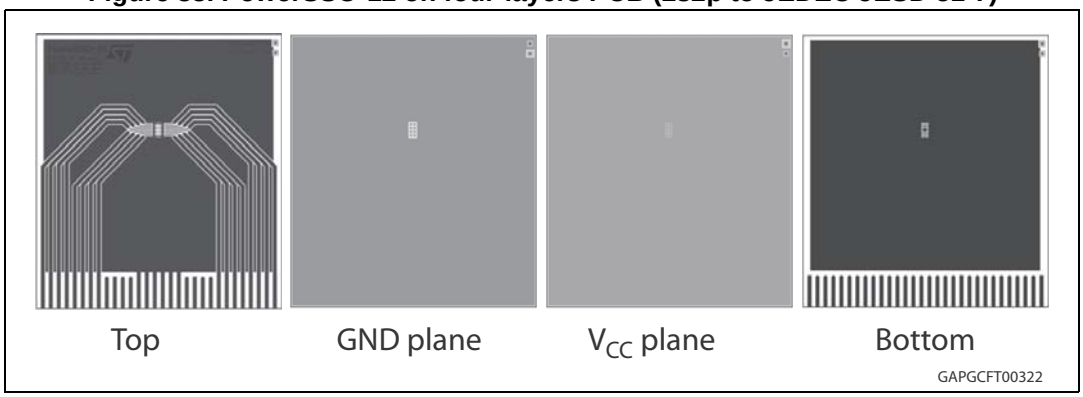



**Table 14. PCB properties**

| Dimension | Value |
|---|---|
| Board finish thickness | 1.6 mm +/- 10% |
| Board dimension | 77 mm x 86 mm |
| Board material | FR4 |
| Copper thickness (top and bottom layers) | 0.070 mm |
| Copper thickness (inner layers) | 0.035 mm |
| Thermal via separation | 1.2 mm |
| Thermal via diameter | 0.3 mm +/- 0.08 mm |
| Copper thickness on via | 0.025 mm |
| Footprint dimension (top layer) | 2.2 mm x 3.9 mm |
| Heatsink copper area dimension (bottom layer) | Footprint, 2 $cm^2$ or 8 $cm^2$ |

**Figure 39. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)**

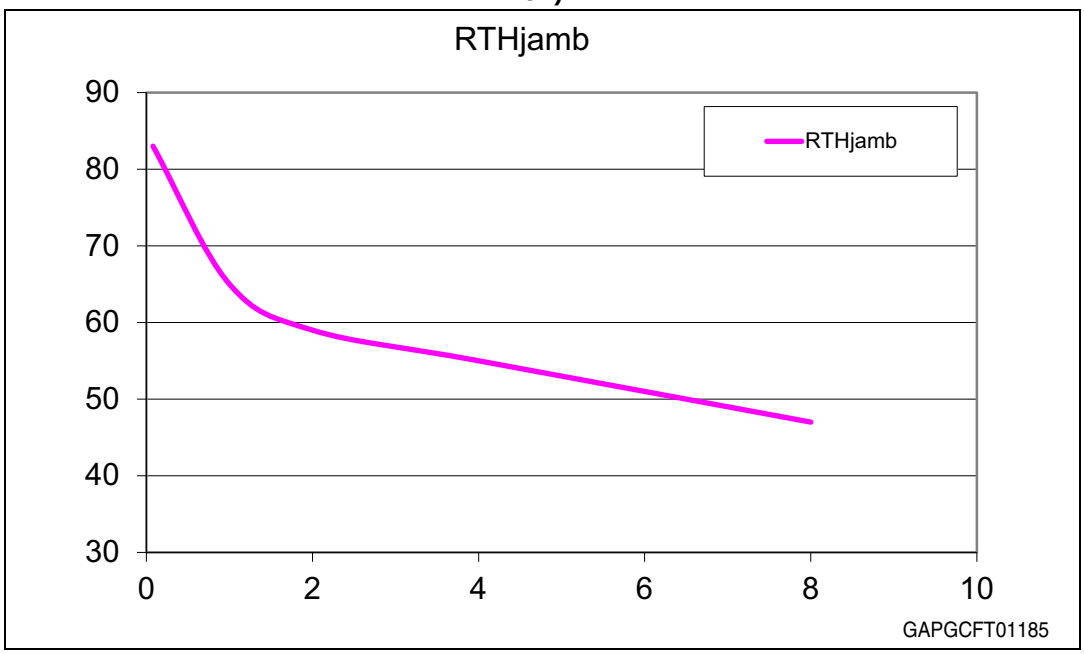
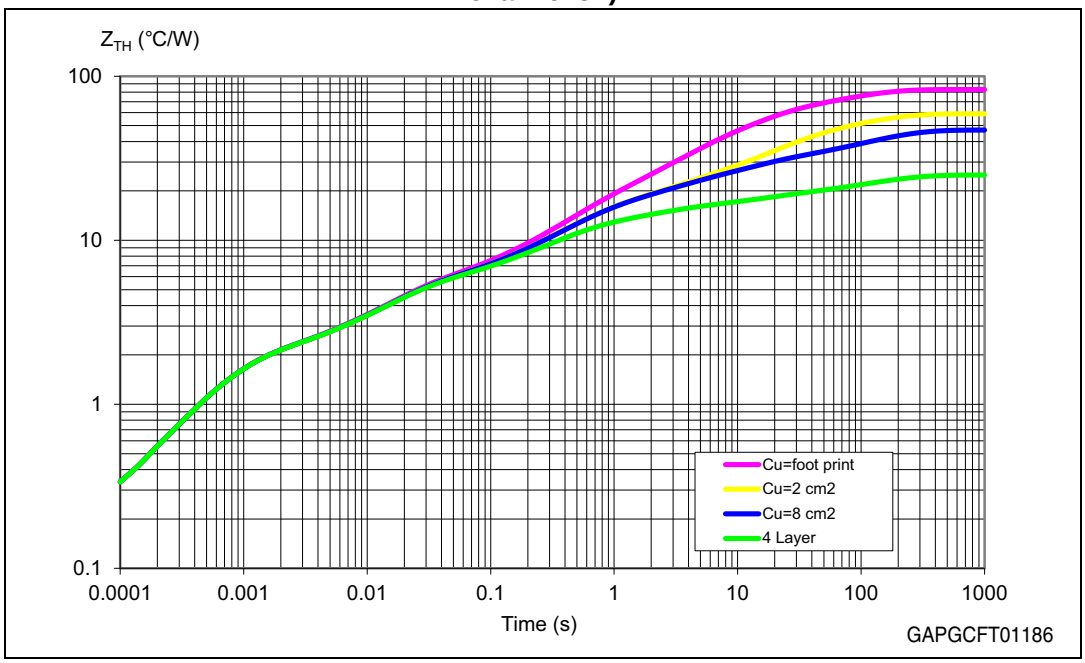



**Figure 40. PowerSSO-12 thermal impedance junction ambient single pulse (one channel on)**

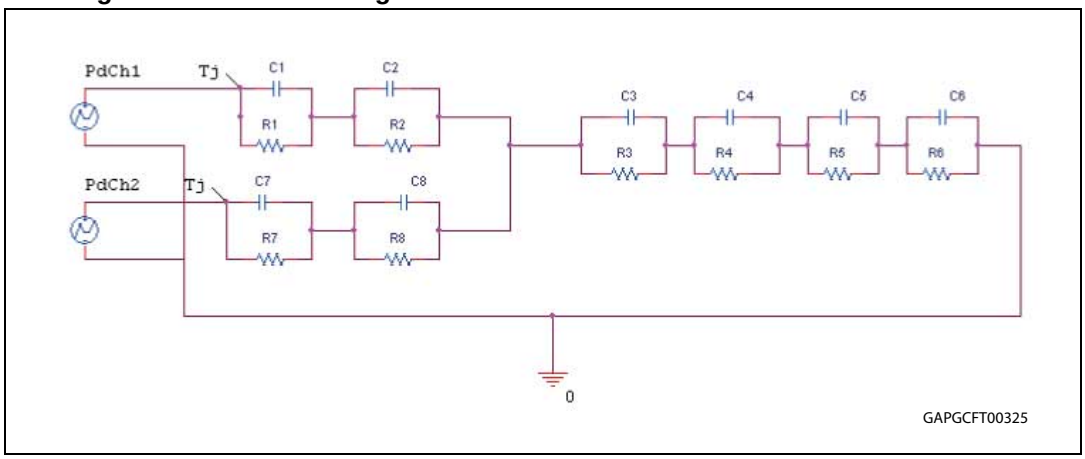



**Equation 3: pulse calculation formula**

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

**Figure 41. Thermal fitting model of a double-channel HSD in PowerSSO-12**




1. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

**Table 15. Thermal parameters**

| Area/island ($cm^2$) | Footprint | 2 | 8 | 4L |
|---|---|---|---|---|
| R1 = R7 (°C/W) | 1.8 | | | |
| R2 = R8 (°C/W) | 3.2 | | | |
| R3 (°C/W) | 8 | 8 | 8 | 6 |
| R4 (°C/W) | 14 | 6 | 6 | 4 |
| R5 (°C/W) | 30 | 20 | 10 | 3 |
| R6 (°C/W) | 26 | 20 | 18 | 7 |
| C1 = C7 (W.s/°C) | 0.00035 | | | |
| C2 = C8 (W.s/°C) | 0.005 | | | |
| C3 (W.s/°C) | 0.05 | | | |
| C4 (W.s/°C) | 0.2 | 0.3 | 0.3 | 0.4 |
| C5 (W.s/°C) | 0.4 | 1 | 1 | 4 |
| C6 (W.s/°C) | 3 | 5 | 7 | 18 |

# 6 Package information

## 6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at *www.st.com*.

ECOPACK® is an ST trademark.

## 6.2 PowerSSO-12 package information

**Figure 42. PowerSSO-12 package dimensions**

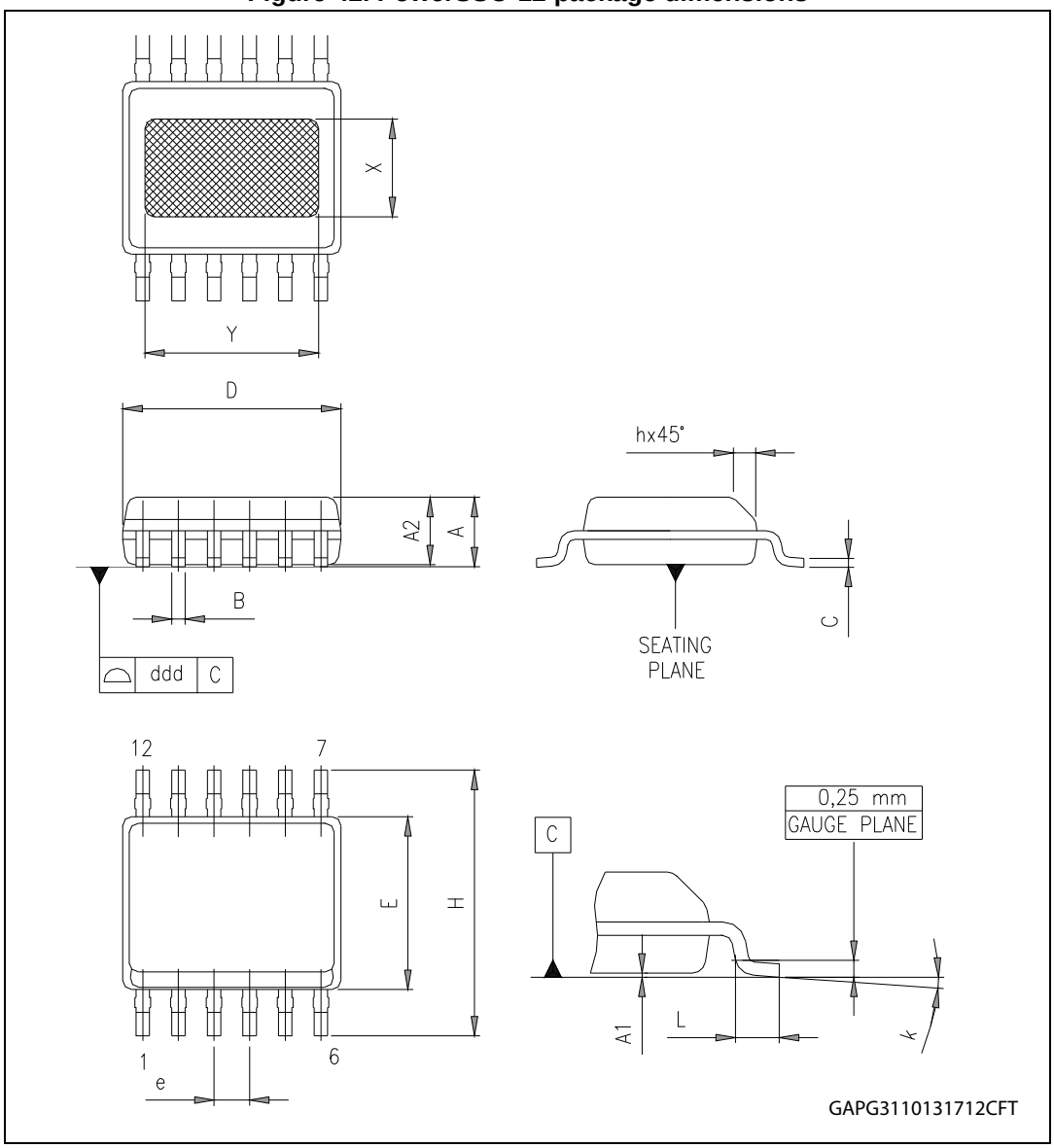


Table 16. PowerSSO-12 mechanical data

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 1.250 | | 1.700 |
| A1 | 0.000 | | 0.100 |
| A2 | 1.100 | | 1.600 |
| B | 0.230 | | 0.410 |
| C | 0.190 | | 0.250 |
| D | 4.800 | | 5.000 |
| E | 3.800 | | 4.000 |
| e | | 0.800 | |
| H | 5.800 | | 6.200 |
| h | 0.250 | | 0.500 |
| L | 0.400 | | 1.270 |
| k | 0° | | 8° |
| X | 2.200 | | 2.800 |
| Y | 2.900 | | 3.500 |
| ddd | | | 0.100 |

# 7 Order codes

Table 17. Device summary

| Package | Order codes | |
|---|---|---|
| | Tube | Tape and reel |
| PowerSSO-12 | — | VND7050AJ12TR-E |

# 8 Revision history

Table 18. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 22-Jan-2014 | 1 | Initial release. |
| 05-Mar-2014 | 2 | Updated *Figure 2: Configuration diagram (top view)* |
| 26-Mar-2015 | 3 | Updated *Table 6: Switching ($V_{CC}$ = 13 V; -40°C < $T_j$ < 150°C, unless otherwise specified)*<br>*Table 9: CurrentSense (7 V < $V_{CC}$ < 18 V; -40°C < $T_j$ < 150°C)*:<br>– $K_{OL}$, $K_{LED}$, $K_0$, $K_1$: updated values<br>Updated *Figure 4: $I_{OUT}/I_{SENSE}$ versus $I_{OUT}$* and *Figure 5: Current sense accuracy versus $I_{OUT}$*<br>Updated *Table 16: PowerSSO-12 mechanical data* and *Table 17: Device summary* |