HI-4850, 4851, 4852

3.0V to 5.5V,Slew-Rate Controlled RS-485/422 Transceivers with Extended Common-Mode Range

April 2017

GENERAL DESCRIPTION

The HI-485x devices are slew-rated controlled TIA-485/TIA-422-B and ISO 8482:1993 compliant transceivers with extended power-supply, temperature and receiver common-mode range for avionic and industrial control applications. The devices can operate over an extended supply (3.0V to 5.5V) and temperature (-55˚C to 125˚C) range. The receiver input common-mode range of [-15, 20]V, and ±24V for the half and full duplex configurations respectively is valid over the full supply and temperature specification. The HI-4850 has a half-duplex configuration, and the HI-4851 and HI-4852 are full-duplex. Slew rates are optimized for data rates below 5 Mbps. The drivers slew-rate control and pre-emphasis reduces high-frequency components in the output signal transitions and also compensates for impedance mismatch. These features provide optimum EMI and jitter performance, essential in EMI sensitive environments and high-integrity data link applications such as in aerospace and industrial controls.

The devices deliver at least ± 1.50V (VDD=3.0V), and ± 2.45V (VDD= 4.5V) output levels at an extended temperature range of -55°C to +125°C into a differential load of 54Ω and 50pF.

The receiver offers true Fail-Safe operation, providing a guaranteed logic high on RO when the bus is open-circuit, short-circuit, or idle (terminated but not driven). The receiver's worst case minimum input resistance is at least 90KΩ, supporting up to 224 nodes

APPLICATIONS

- Extended Temperature Range RS-485/422 Networks
- Process Control and Factory Automation
- EMI Emission Sensitive Avionics
- Industrial Field Bus Networks
- Networks requiring extended common-mode range

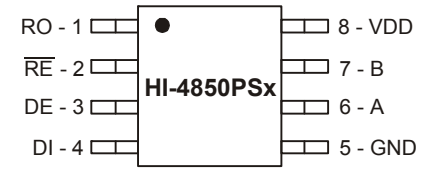
Device Selection Table			
Part Number	**Half/Full Duplex**	**Data Rate (Mbps)***	**Package**
HI-4850	Half	≤ 5.0	8-pin SOIC
HI-4851	Full	≤ 5.0	8-pin SOIC
HI-4852	Full	≤ 5.0	14-pin SOIC 16-pin QFN

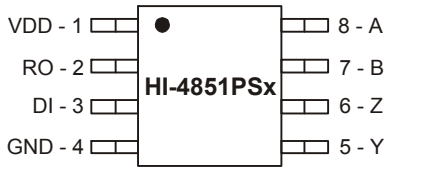
* For RS-485 Transceivers optimized for data rates up to 20Mbps please refer to the HI-4853 data sheet.

FEATURES

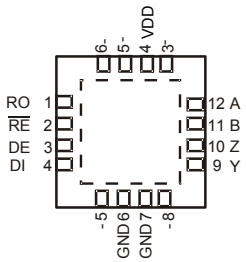
- Slew Rate Control and Pre-Emphasis for superior EMI
- Extended Power Supply Operating Range 3.0V to 5.5V
- Extended Receiver Common-Mode Range:
  - **-15.0V to 20.0V Half-Duplex**
  - **±24V Full-Duplex**
- ESD Protection
  - 16KV HBM (Bus Pins)
  - 8KV HBM (Logic Pins)
- 5 Mbps Date Rate up to 100 ft. CAT-5 UTP
- 2 Mbps Data Rate up to 1000 ft. CAT-5 UTP
- Current Limiting Protection
- Extended Temperature Range -55°C to 125°C
- Industry Standard 75176 Pin-out

PIN CONFIGURATIONS (Top Views)



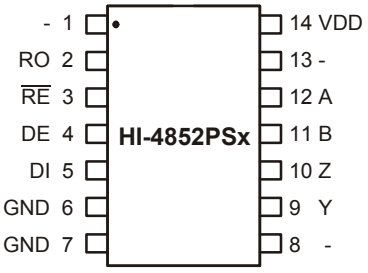


8-Pin Plastic SOIC package (Narrow Body)



HI-4852PCx

16- pin 4mm x 4mm Chip-scale package



14-Pin Plastic SOIC package (Narrow Body)

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
RO	OUTPUT	Receiver Output. If V_{ID} ≥ -50mV, then RO is high. If V_{ID} < -150mV then RO is low. If the bus is shorted, open or terminated but not driven by another terminal, RO will be high.
$\overline{RE}$	INPUT	Receiver Enable. $\overline{RE}$= Low enables the receiver. $\overline{RE}$ High forces the receiver output (RO) into a high impedance state. Internal 450KΩ pull-down resistor
DE	INPUT	Driver Enable. DE = high enables the driver. DE = low will force the driver output into a high impedance state and the device will function as a line receiver if $\overline{RE}$ is also low. Internal 450KΩ pull-up resistor
DI	INPUT	Driver Input. Forces the logic state of the Driver's output, if Driver is enabled. Internal 450KΩ pull-up resistor
GND	POWER	Chip ground, 0V Supply
A, Y	ANALOG I/O	Non-inverting Receiver Input / Driver Output.
B, Z	ANALOG I/O	Inverting Receiver Input / Driver Output.
VDD	POWER	Positive Supply: 3.0V ≤ VDD ≤ 5.5V

TX FUNCTION TABLE

TRANSMITTING					
INPUTS			LINE CONDITION	OUTPUTS	
$\overline{RE}$	DE	DI		B	A
X	1	1	Transmit logic high	0	1
X	1	0	Transmit logic low	1	0
0	0	X	Disable	Hi-Z	Hi-Z
1	0	X	Shutdown	Hi-Z	Hi-Z

RX FUNCTION TABLE

RECEIVING				
INPUTS		BUS PINS $V_{ID} = V_A - V_B$	OUTPUT RO	OPERATION
$\overline{RE}$	DE			
0	0	-150mV < V_{ID} < -50mV	X	Undefined Input
0	X	-50mV ≤ V_{ID}	1	Receiver logic high
0	X	V_{ID} ≤ -150mV	0	Receiver logic low
0	0	Open or Shorted	1	Default
0	0	Idle and terminated	1	Default
1	1	X	Hi-Z	Disabled
1	0	X	Hi-Z	Shutdown

Typical Operating Circuit

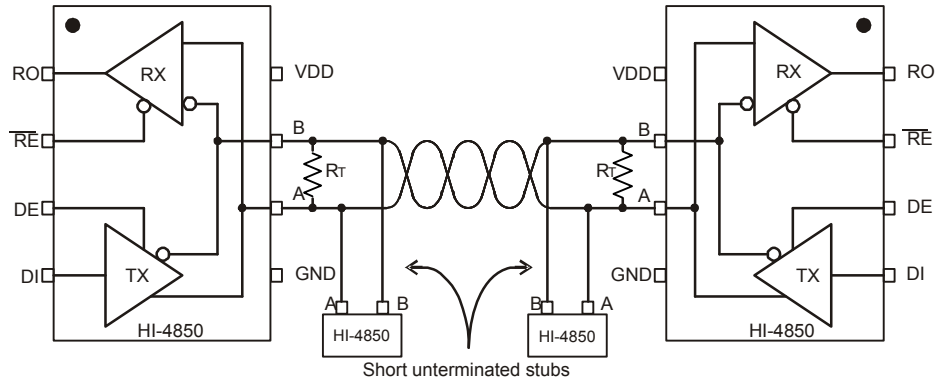


Figure 1 - Typical half-duplex configuration

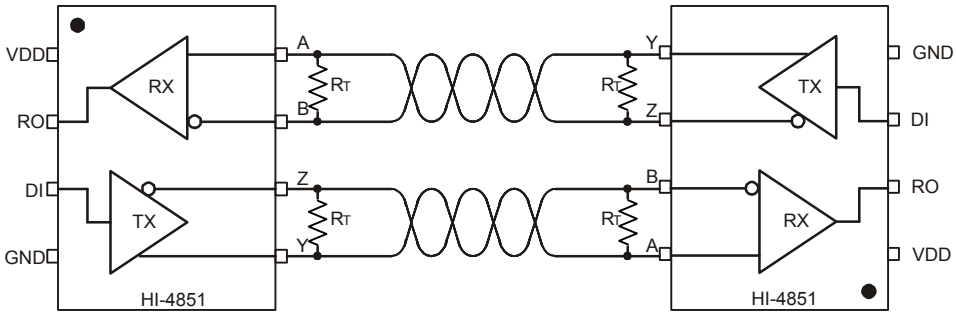


Figure 2 - Typical full-duplex 8-pin configuration

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND = 0V)

Supply Voltage, VDD:.....7 V
Control Input Currents: .....-100mA to 100mA
Digital Input Voltages (DI, DE, $\overline{RE}$):.....-0.5V to VDD + 0.5V
Bus Voltage (AY, BZ):.....±25V
Digital Output Voltage (RO):.....-0.5V to V + 0.5V
Short-Circuit Duration, Driver (V: ±15V)..... ∞
ESD (Human Body Model):
AY, BZ,VDD,GND pins:.....±16KV
DI, DE, $\overline{RE}$, RO pins:.....±8KV

Operating Temperature Range:(Industrial).....-40°C to +85°C
(Hi-Temp).....-55°C to +125°C

Internal Power Dissipation:.....900mW

Storage Temperature Range: .....-65°C to +150°C

Solder Temperature: (Reflow)..... +260°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFIED OPERATING CONDITIONS

PARAMETERS	SYMBOL	CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Supply Voltage	V_{DD}		3.0	3.3 / 5.0	5.5	V
Temperature	T		-55		125	˚C
TX Common-Mode Bus Loading	V_{OCM}	See Figure 4	-7		12	V
RX Input Common-Mode Voltage	V_{ICM}	Half-Duplex	-16		20	V
Differential Load Resistance	R_L		54	60	∞	Ω
Differential Load Capacitance	C_L			100		pF
Digital Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$	70			$\%V_{DD}$
Digital Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$			30	$\%V_{DD}$
Digital Input Current high	I_{IH}	DE, DI, $V_{IH} = V_{DD}$			1	µA
Digital Input Pull-Down Current	I_{PD}	$\overline{RE}$, $V_{IH} = V_{DD}$	6		18	µA
Digital Input Current low	I_{IL}	$\overline{RE}$, $V_{IH} = 0$	-1			µA
Digital Input Pull-Up Current	I_{PU}	DE, DI, $V_{IH} = 0V$	-18		-6	µA

DRIVER DC ELECTRICAL CHARACTERISTICS

VDD = 3.0V to 3.6V or 4.5V to 5.5V; T = -55˚C to 125˚C; MIN and MAX values are at range boundaries

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Differential Output Voltage with no load	$\|V_{OD1}\|$	$R_L = ∞$	3	V_{DD} -0.1		V_{DD}	V_{DD} -0.1		V_{DD}	V
Differential Output Voltage into load with no common-mode voltage	$\|V_{OD2}\|$	$R_L = 54Ω$, $C_L = 50pF$	3	1.5		3.0	2.45		4.0	V
Differential Output Voltage into load with applied common-mode voltage	$\|V_{OD3}\|$	-7V ≤ V_{OCM} ≤ 12V T_A = 25ºC	4	1.5		3.0	2.45		4.0	V
Differential Output Over/Under Shoot						5.5			3.2	$\%V_{OD}$
Change in Differential Output Voltage between logic states	ΔV_{OD}	$R_L = 54Ω$, $C_L = 50pF$	3	-125		125	-125		125	mV
Output Common-Mode Voltage	V_{OCM}	$R_L = 54Ω$, $C_L = 50pF$	4	1.40	1.60	2.0	2.15	2.45	3.0	V
Change in output Common-Mode Voltage between logic states	ΔV_{OCM}	$R_L = 54Ω$, $C_L = 50pF$	4	-125		125	-150		150	mV
Bus Pin Leakage Current (High-Z Power On)	I_{OHZ1}	DE=0, -15V≤ VOCM ≤ 15V DE=0, -12V≤ VOCM ≤ 15V		-200		200	-200		200	µA
Bus Pin Leakage Current (Power Off)	I_{OHZ2}	V_{OCM} = ±15V		-200		200	-200		200	µA
Peak Short Circuit Current	I_{SCPK}	DE = V_{DD}, Bus Pin = ±15		-230		230	-250		250	mA
Steady State Short Circuit Current	I_{SC}	DE = V_{DD}, Bus Pin = ±15		0		50	0		50	µA
Differential Output Capacitance	C_{OD}	DE = 0				16			16	pF
Static Supply Current	I_{DD}	DE=V_{DD}, RE=0, R_L=∞			8	10		10	12	mA
Supply Current (Shutdown)	I_{DDQ}	DE=0, RE=V_{DD}, R_L=∞			90	110		100	400	µA

DRIVER SWITCHING CHARACTERISTICS

VDD = 3.0V - 3.6V or 4.5V - 5.5V as noted , Operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Low - to - High	t_{PDR}	R_L = 54Ω. C_L=50pF	5 & 6	110	145	200	108	150	205	ns
Propagation Delay High - to - Low	t_{PDF}	R_L = 54Ω, C_L=50pF	5 & 6	110	145	200	108	150	205	ns
Differential Rise Time	t_r	R_L = 54Ω, C_L=50pF	5 & 6	90	105	120	115	135	155	ns
Differential Fall Time	t_f	R_L = 54Ω, C_L=50pF	5 & 6	90	105	120	115	135	125	ns
Output Pulse Skew	t_{MSK}	R_L = 54Ω, C_L=50pF	5 & 6		2	8		2	8	ns
Driver Enable to Output High	t_{ZH}	R_L = 500Ω, C_L=50pF	7		95	120		90	117	ns
Driver Enable to output Low	t_{ZL}	R_L = 500Ω, C_L=50pF	7		95	120		90	117	ns
Driver Disable from Output High	t_{HZ}	R_L = 500Ω, C_L=50pF	7		20	33		18	30	ns
Driver Disable from Output Low	t_{LZ}	R_L = 500Ω, C_L=50pF	7		20	33		18	30	ns
Shutdown to Active Output Delay	t_{ON}	R_L = 500Ω, C_L=50pF	7			10			10	µs
Shutdown Delay	t_{OFF}					10			10	µs

RECEIVER DC ELECTRICAL CHARACTERISTICS

VDD = 3.0V - 3.6V or 4.5V - 5.5V as noted , Operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input Threshold Voltage	V_{TH}	-15 ≤ V_{ICM} ≤ +20		-200	-100	-50	-200	-100	-50	mV mV
Input Hysteresis	V_{HYS}	V_{ICM} = 0V		17	28	33	17	28	33	mV
Input Resistance	R_{IN}	-15 ≤ V_{ICM} ≤ +20		80	92		80	92		KΩ KΩ
RO Output High Level	V_{OH}	V_{ICM} = +200mV I_{OUT} = -3.0mA		90%			90%			V_{DD}
RO Output Low Level	V_{OL}	V_{ICM} = -200mV I_{OUT} = +3.0mA				10%			10%	V_{DD}
RO Output Hi-Z Leakage Current	I_{OZH}	0V ≤ V_{RO} ≤ V_{DD}		-1		1	-1		1	µA

RECEIVER SWITCHING CHARACTERISTICS

VDD = 3.0V - 3.6V or 4.5V - 5.5V as noted , Operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	FIGURE	VDD = 3.3V ± 10%			VDD = 5.0V ± 10%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Low - to - High	t_{RPDR}	V_{ID} = +1.5V, C_L=15pF	8	20	26	32	20	26	32	ns
Propagation Delay High - to - Low	t_{RPDF}	V_{ID} = -1.5V, C_L=15pF	8	20	26	32	20	26	32	ns
RO Output Rise Time	t_{Rr}	V_{ID} = +1.5V, C_L=15pF	8	1.1	1.9	3.3	1.1	1.9	3.3	ns
RO Output Fall Time	t_{Rf}	V_{ID} = -1.5V, C_L=15pF	8	1.1	1.9	3.3	1.1	1.9	3.3	ns
Output Pulse Skew	t_{RMSK}	V_{ID} = +1.5V, C_L=15pF	8		0.8	1.6		0.8	1.6	ns
Receiver Enable to RO Output High	t_{RZH}	R_L = 1KΩ, C_L=15pF	9		12	16		12	16	ns
Receiver Enable to output Low	t_{RZL}	R_L = 1KΩ, C_L=15pF	9		12	16		12	16	ns
Receiver Disable from Output High	t_{RHZ}	R_L = 1KΩ, C_L=15pF	9		6	10		6	10	ns
Receiver Disable from Output Low	t_{RLZ}	R_L = 1KΩ, C_L=15pF	9		6	10		6	10	ns
Shutdown to RO Active Output Delay	t_{RON}	R_L = 1KΩ, C_L=15pF	9			5			5	µs
Shutdown Delay to RO HiZ	t_{ROFF}	R_L = 1KΩ, C_L=15pF	9		60	100		60	100	ns

TEST CIRCUITS

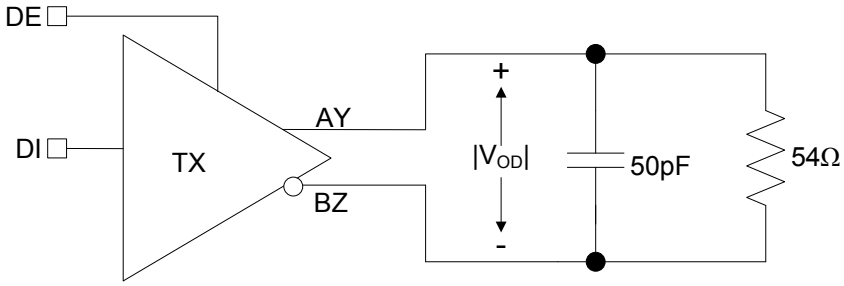


Figure 3 - Driver DC Characteristics (V_{OD1}, V_{OD2}, and ΔV_{OD})

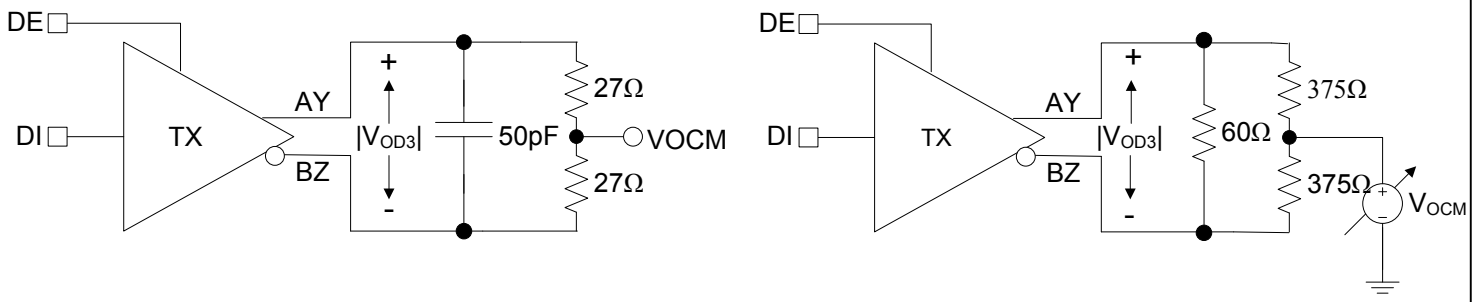


Figure 4 - Driver DC Characteristics with and without Common-Mode Loading (V_{OCM}, V_{OD3}, and ΔV_{OD})

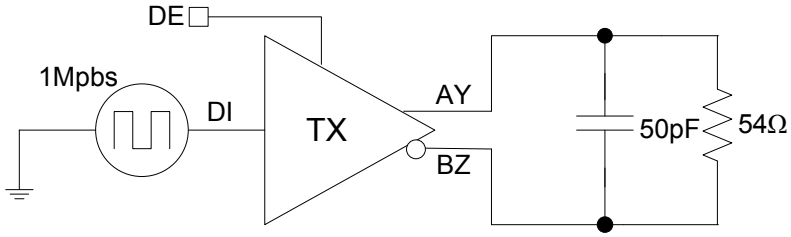


Figure 5 - Driver Switching Characteristics (t_{PDR}, t_{PDF}, t_r and t_f)

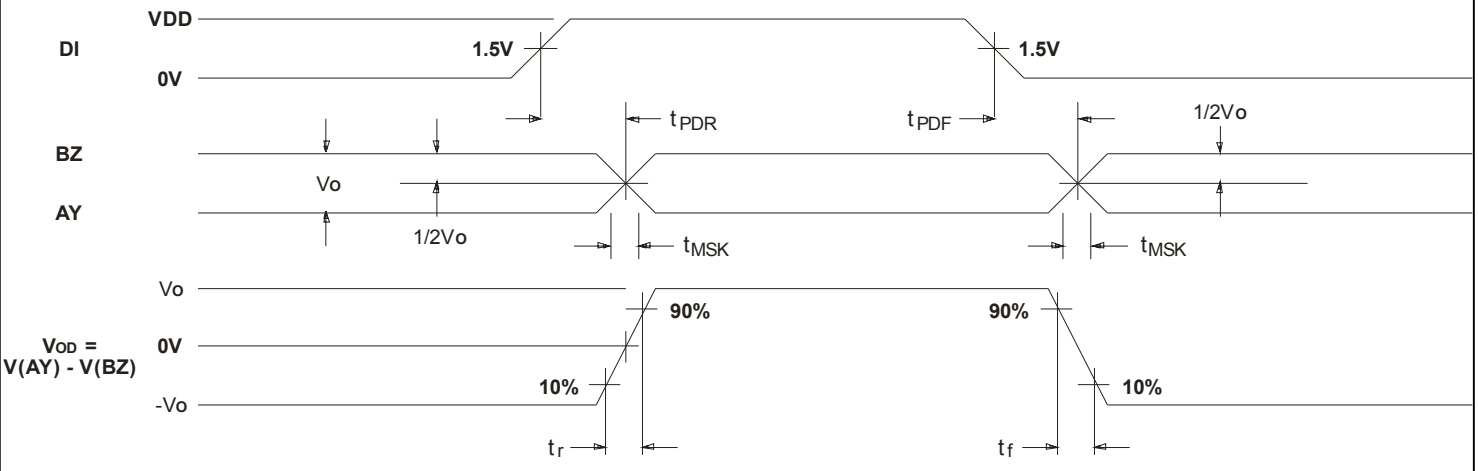


Figure 6. Driver Switching Waveforms

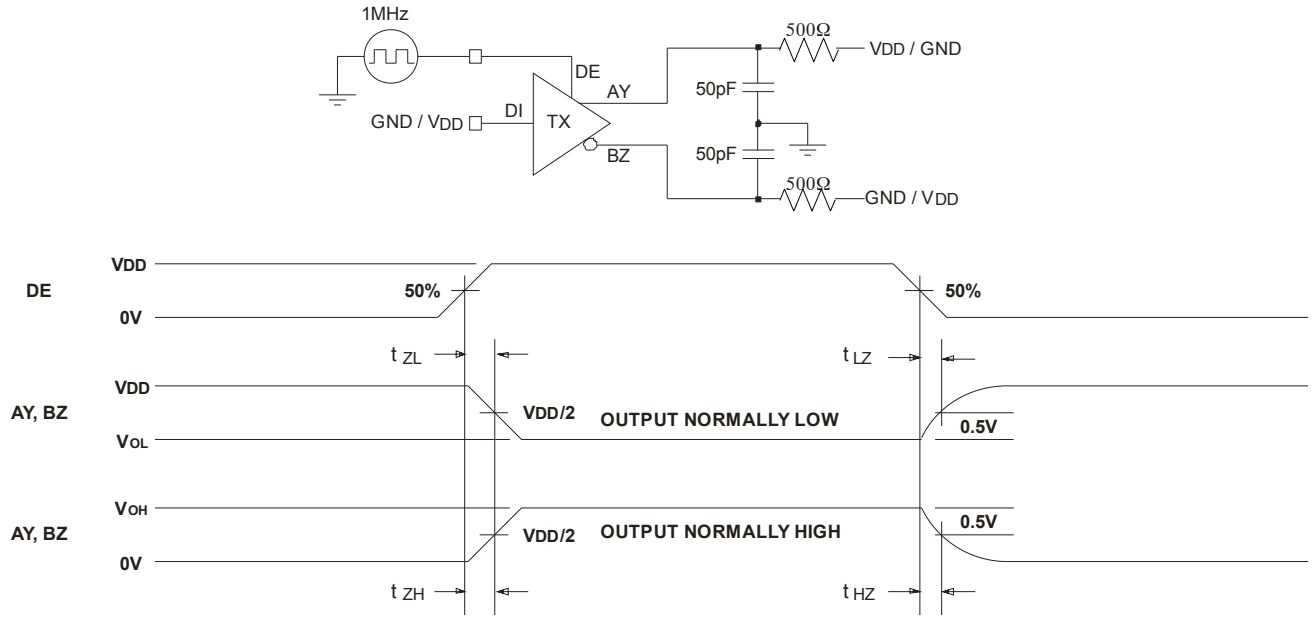


Figure 7. **Driver Enable / Disable Switching**

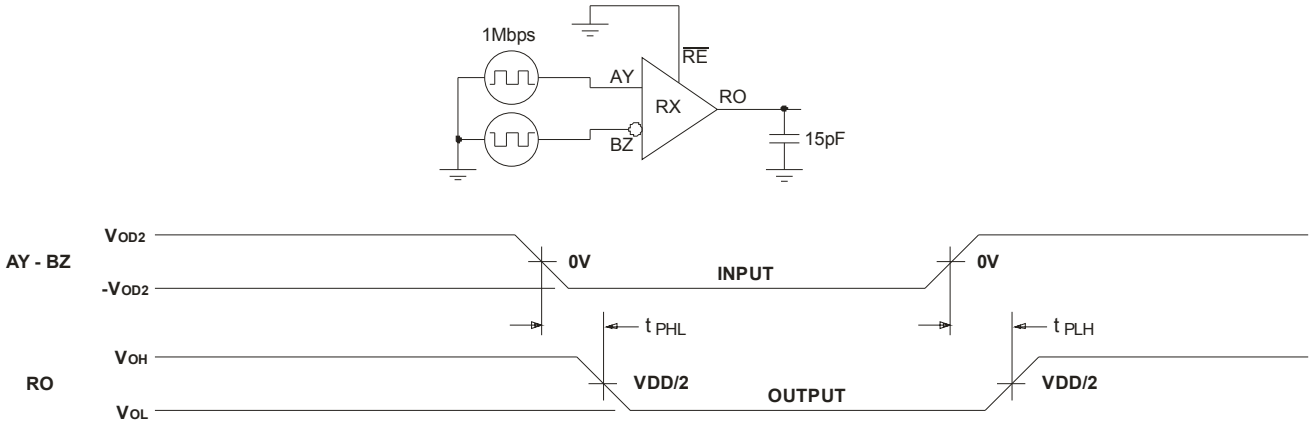


Figure 8. **Receiver Propagation Delays**

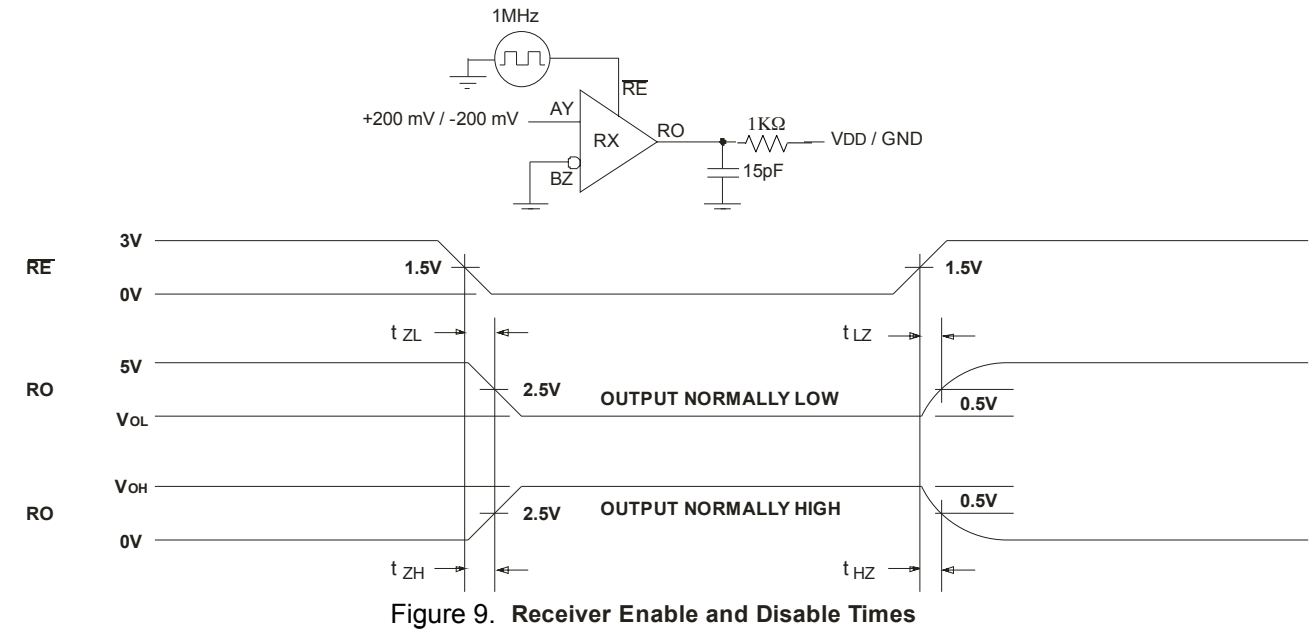
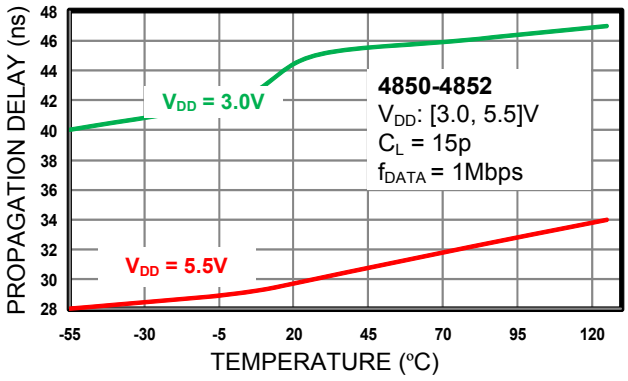


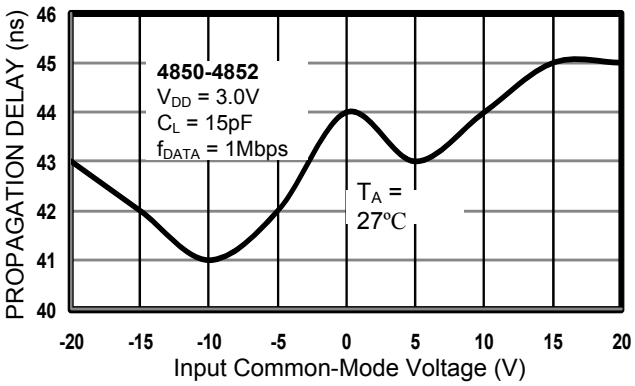
Figure 9. **Receiver Enable and Disable Times**

PERFORMANCE CHARACTERISITICS OVER SUPPLY AND TEMPERATURE
HI-4850/52

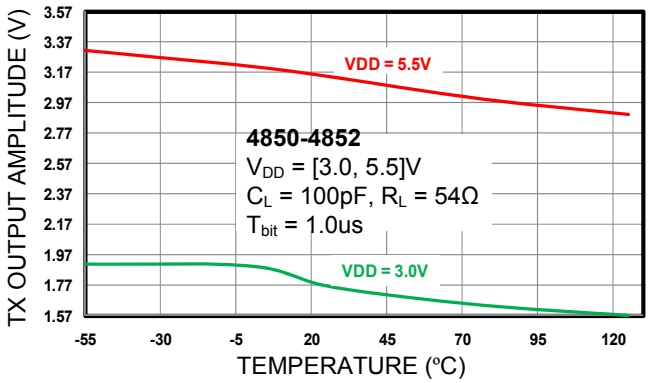
RX PROPAGATION DELAY vs. TEMPERATURE



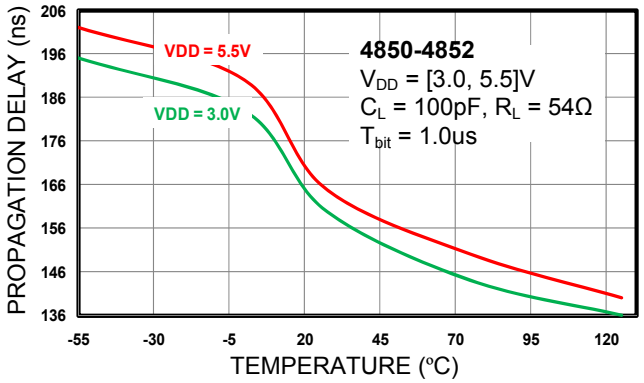
RX PROP DELAY vs. INPUT COMMON-MODE



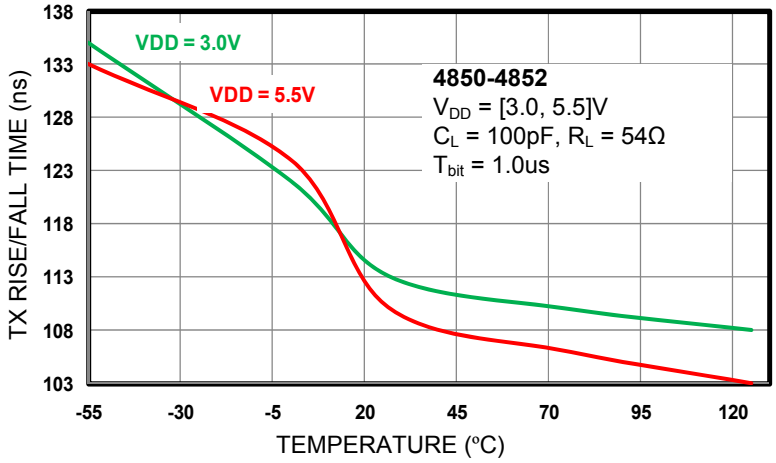
TX DIFFERENTIAL ZERO TO PEAK AMPLITUDE vs. TEMPERATURE



TX PROPAGATION DELAY vs. TEMPERATURE

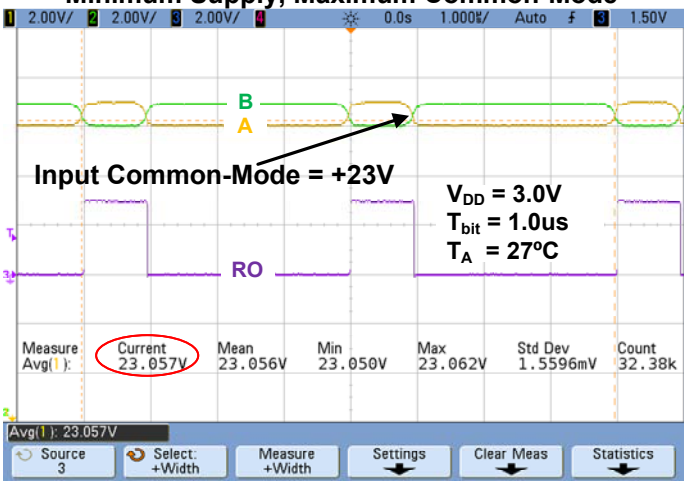


TX Rise/Fall Time vs. TEMPERATURE

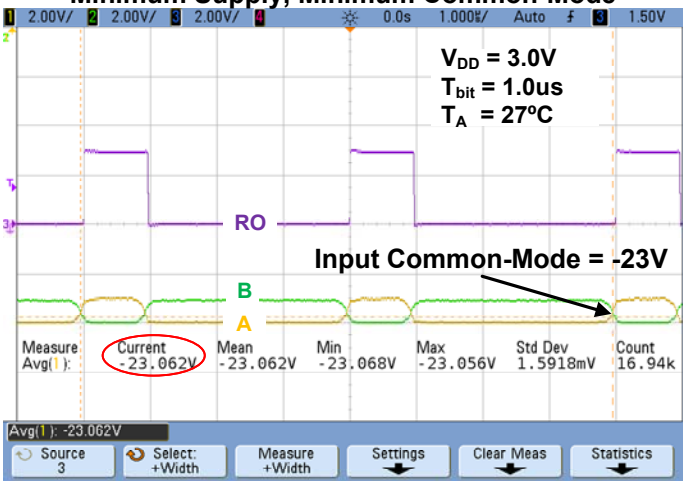


Full Duplex Receiver Typical Performance Characteristics
HI-4851/52

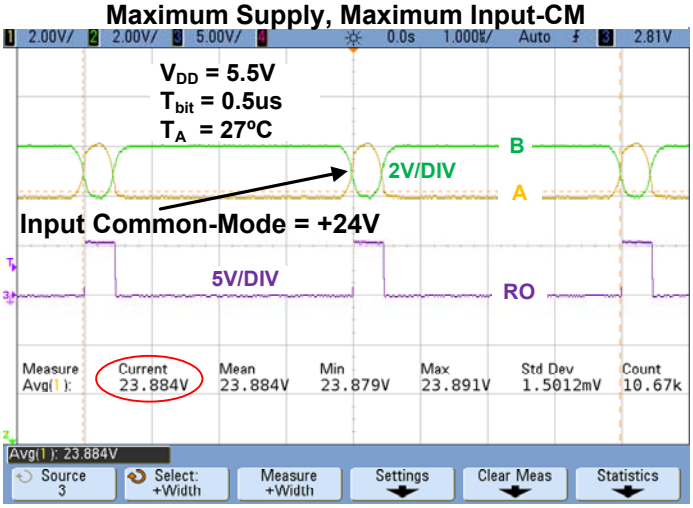
RX Extended Common-Mode Range: Minimum Supply, Maximum Common-Mode



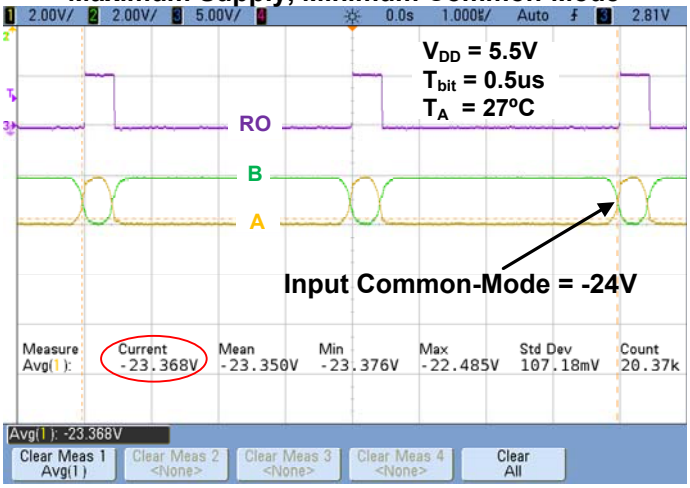
RX Extended Common-Mode Range: Minimum Supply, Minimum Common-Mode



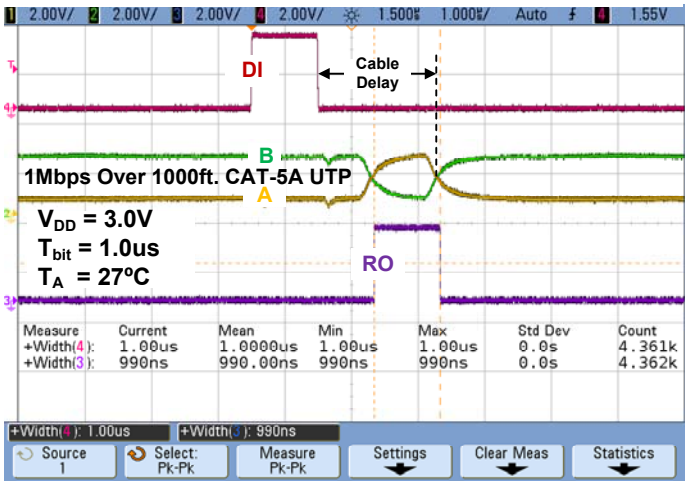
RX Extended Common-Mode Range: Maximum Supply, Maximum Input-CM



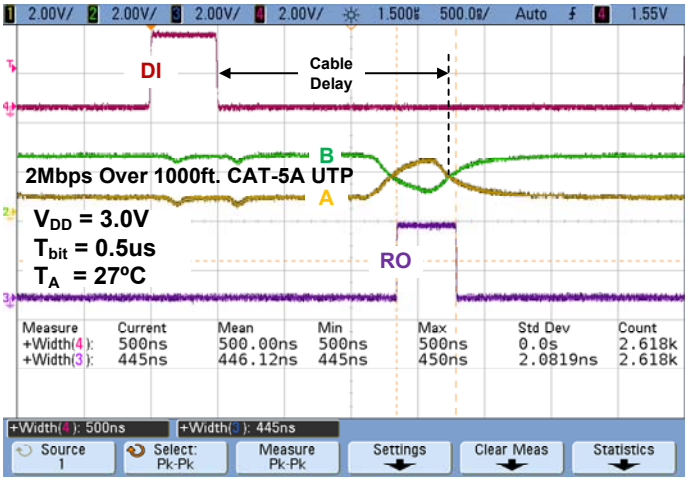
RX Extended Common-Mode Range: Maximum Supply, Minimum Common-Mode



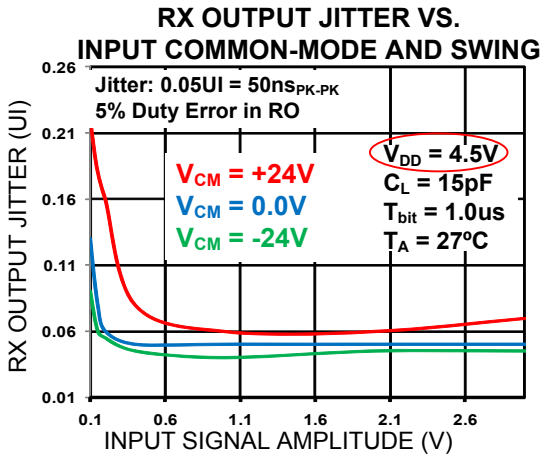
1Mbps Data Pulse Over 1000ft CAT-5 UTP



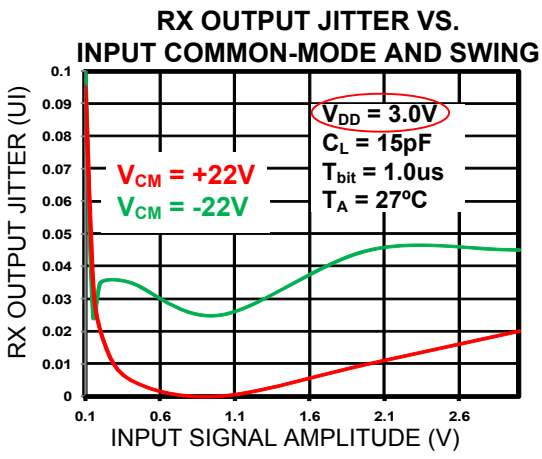
2Mbps Data Pulse Over 1000ft CAT-5 UTP



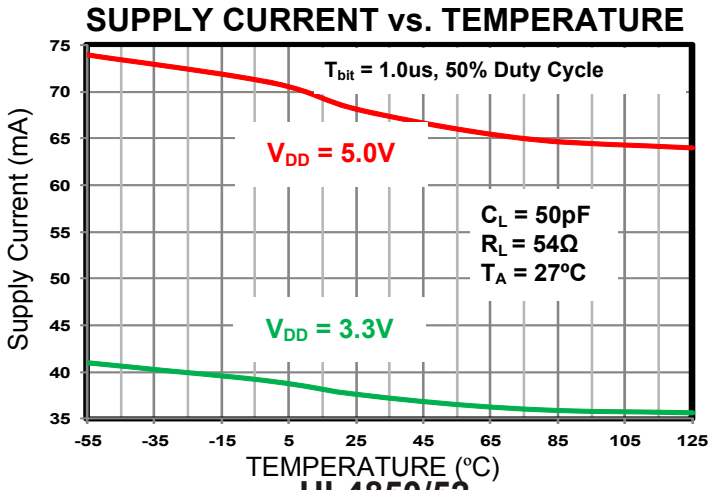
TYPICAL TRANCEIVER PERFORMANCE CHARACTERISITICS



HI-4851/52

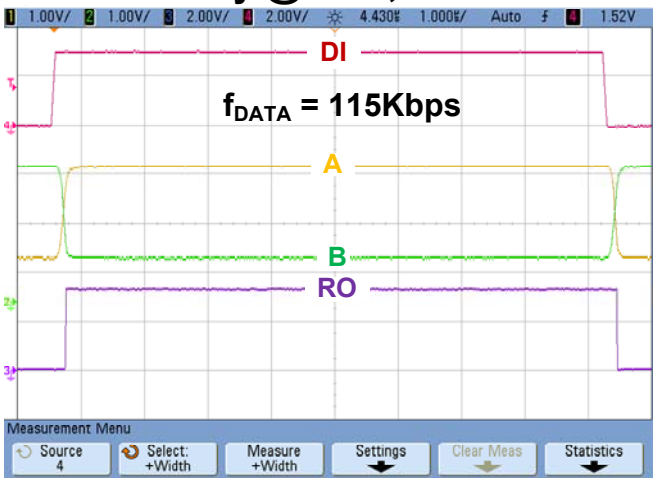


HI-4851/52



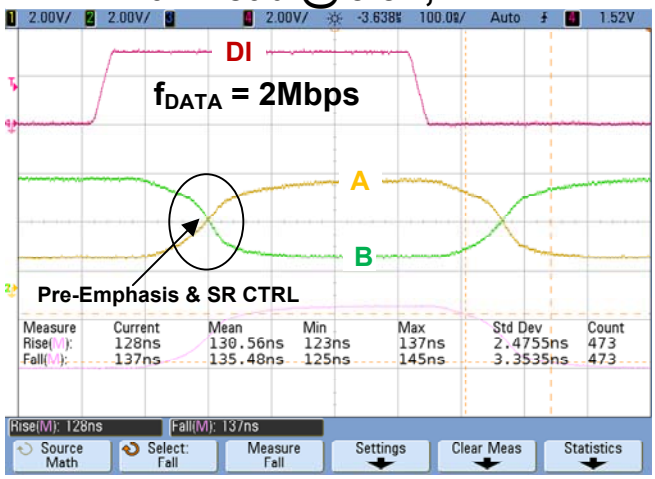
HI-4850/52

Typical TX/RX Propagation Delay @ 3.3V, 27 ºC



HI-4850/52

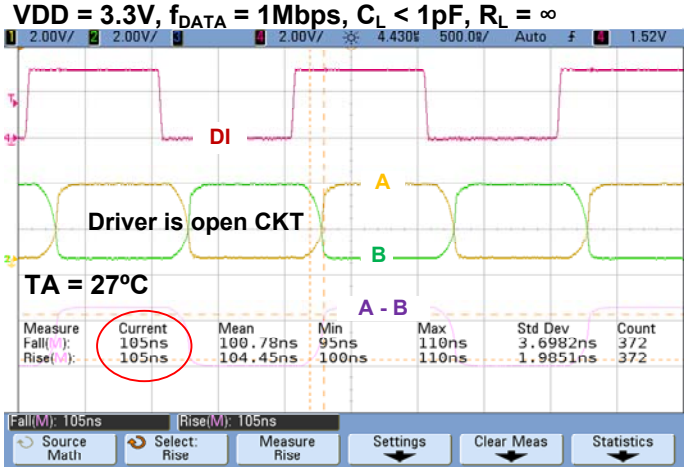
Typical TX Rise/Fall Time Max Load @ 3.3V, 27 ºC



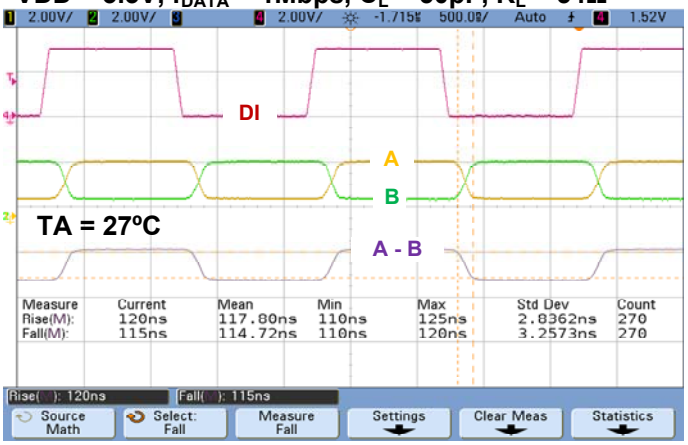
HI-4850/52

TYPICAL PERFORMANCE CHARACTERISITICS
HI-4850/52

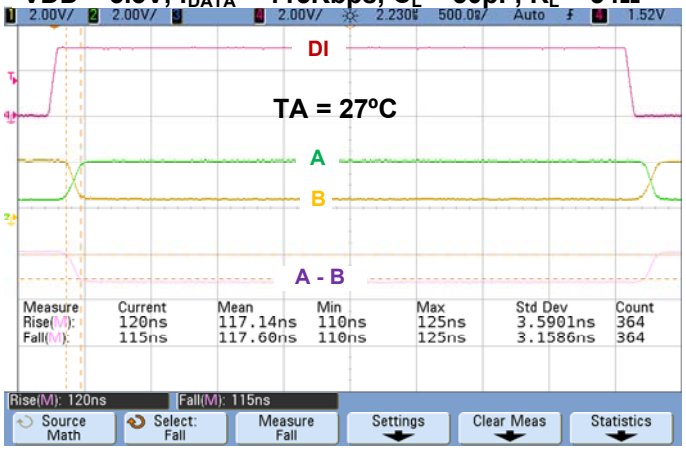
TX Slew-Rate Controlled Output Characteristics:
VDD = 3.3V, f_{DATA} = 1Mbps, C_L < 1pF, R_L = ∞



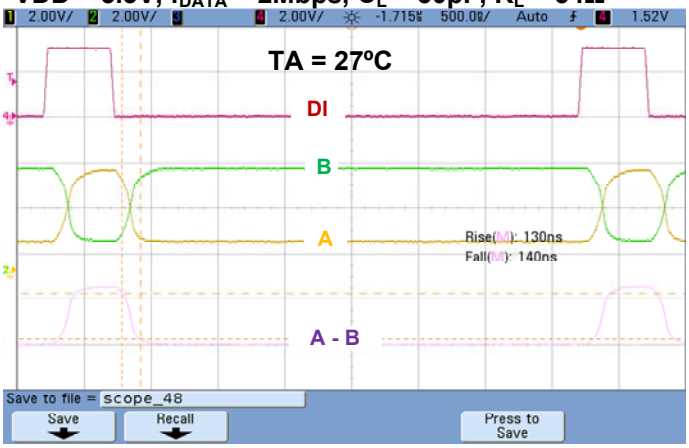
TX Slew-Rate Controlled Output Characteristics:
VDD = 3.3V, f_{DATA} = 1Mbps, C_L = 50pF, R_L = 54Ω



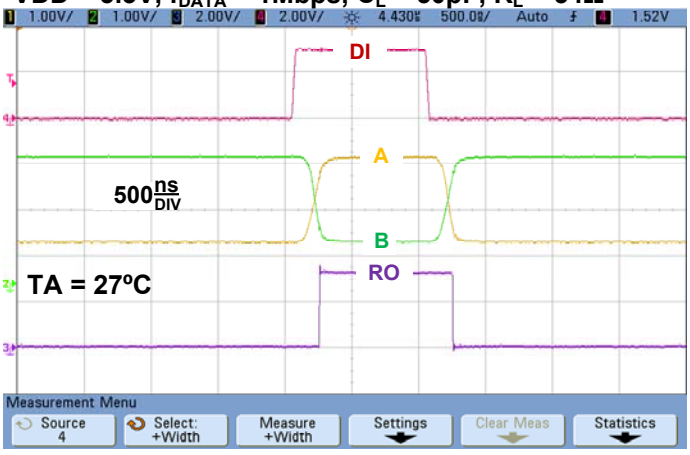
TX Low Speed Output Characteristics:
VDD = 3.3V, f_{DATA} = 115Kbps, C_L = 50pF, R_L = 54Ω



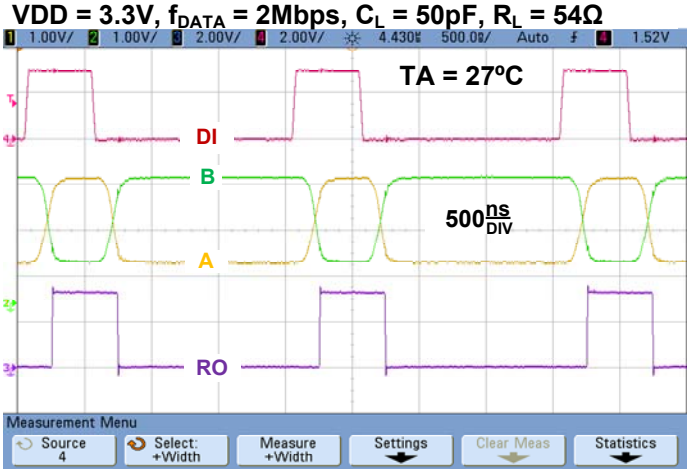
TX High Speed Output Characteristics:
VDD = 3.3V, f_{DATA} = 2Mbps, C_L = 50pF, R_L = 54Ω



TX / RX Propagation Delay:
VDD = 3.3V, f_{DATA} = 1Mbps, C_L = 50pF, R_L = 54Ω



TX / RX Propagation Delay:
VDD = 3.3V, f_{DATA} = 2Mbps, C_L = 50pF, R_L = 54Ω



ORDERING INFORMATION

HI - 485x xx x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PC	16 PIN PLASTIC 4 x 4 mm CHIP SCALE (16PCS) (HI-4852 only. No M-flow)
PS	8 PIN PLASTIC NARROW BODY SOIC (8HN) (HI-4850, HI-4851)
PS	14 PIN PLASTIC NARROW BODY SOIC (14HN) (HI-4852 only)
CR	8 PIN CERDIP (8D) not available Pb-free (HI-4850, HI-4851)

PART NUMBER	FUNCTION
4850	HALF DUPLEX TRANSCEIVER
4851	FULL DUPLEX TRANCEIVER ALWAYS ENABLED
4852	FULL DUPLEX TRANSCEIVER WITH ENABLE PINS

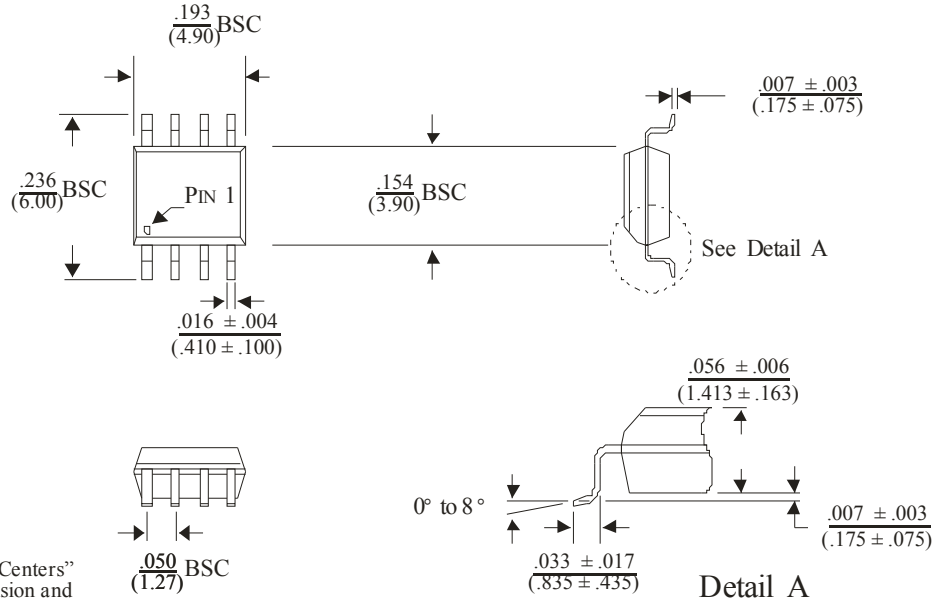
REVISION HISTORY

Revision	Date	Description of Change
DS4850, Rev New	10/12/2011	Initial Release
Rev. A	3/15/2012	Added characterization data. Fixed errors in V_{IL} and V_{IH} values.
Rev. B	8/2/2012	Updated Rx Function Table rows 2 and 3 on p. 2 for DE = X. Updated package drawings for SOIC-8 (8HN), QFN-16 (16PCS) and SOIC-14 (14HN) packages.
Rev. C	03/13/2013	Correct typo on nRE pull-up resistor (should be pull-down). Update Digital Input pull-up/pull-down current. Update typo in Figure 4 resistors. Update solder temperature (reflow) in Max. Ratings
Rev. D	04/18/2017	Remove redundant Control Input Voltages from Absolute Maximum Ratings (same parameter as Digital Input Voltages).

8-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

inches (millimeters)

Package Type: 8HN

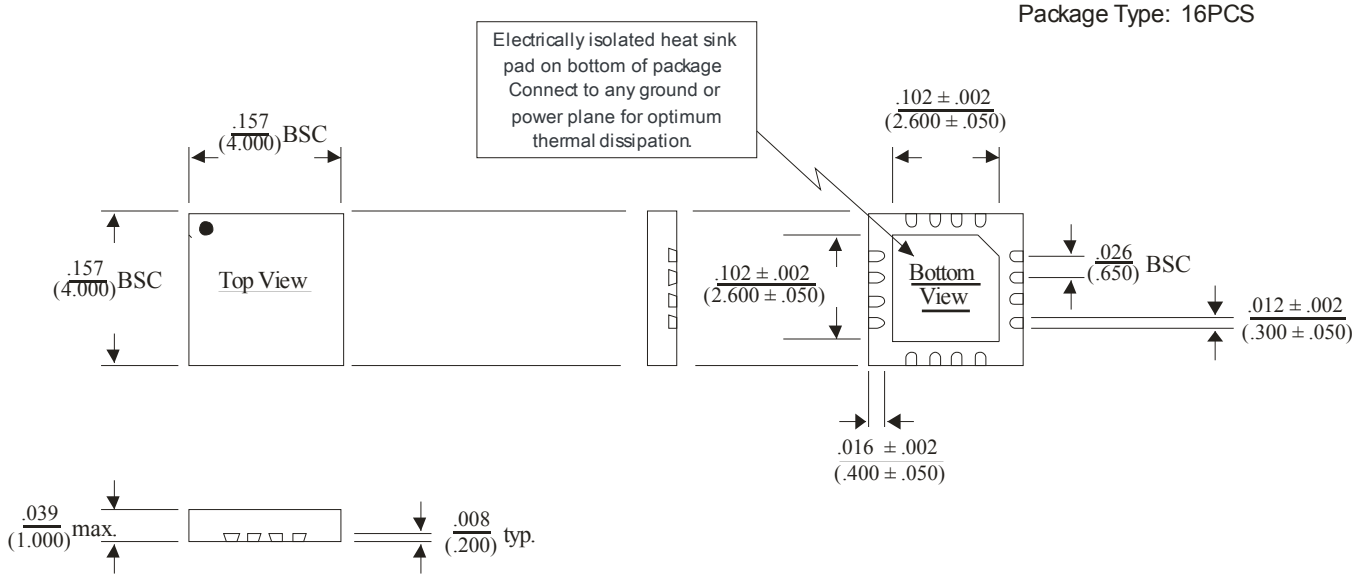


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

16-PIN PLASTIC CHIP-SCALE PACKAGE

inches (millimeters)

Package Type: 16PCS

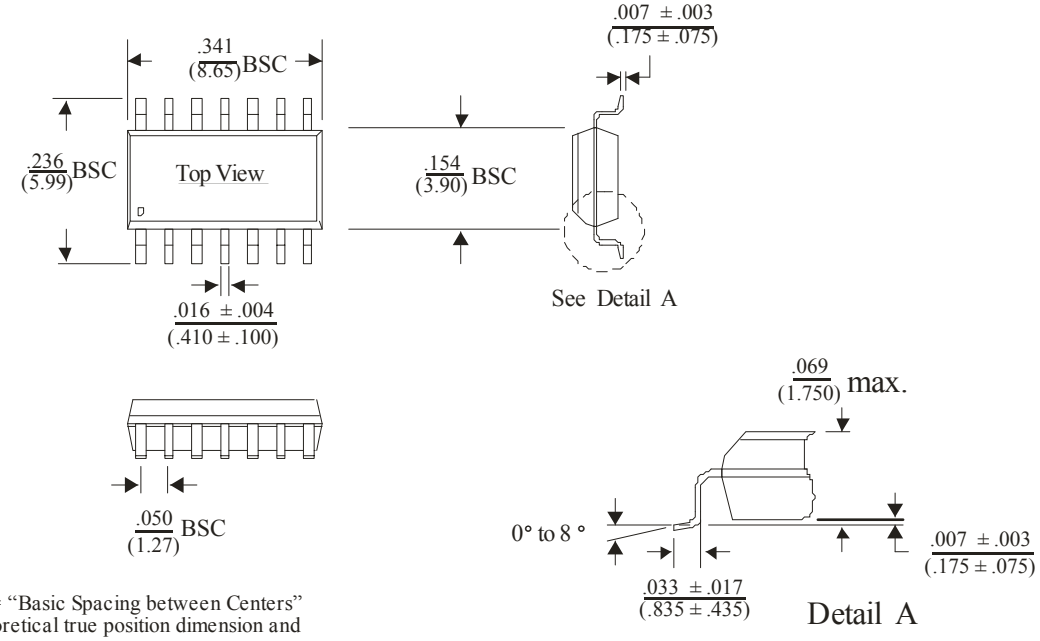


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

14-PIN PLASTIC SMALL OUTLINE (SOIC) - NB
(Narrow Body)

inches (millimeters)

Package Type: 14HN

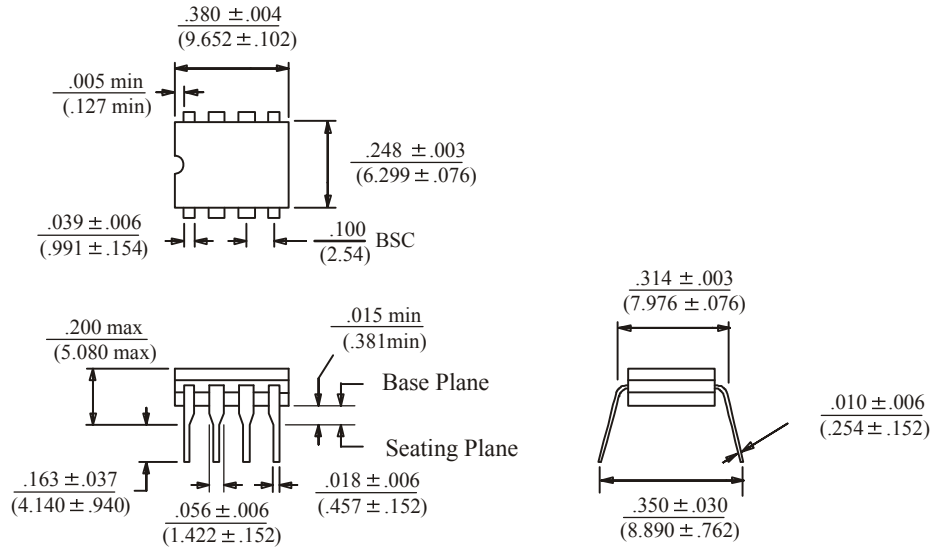


BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

8-PIN CERDIP

inches (millimeters)

Package Type: 8D



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)