MC74VHC245

Octal Bus Buffer/Line Driver

The MC74VHC245 is an advanced high speed CMOS octal bus transceiver fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It is intended for two−way asynchronous communication between data buses. The direction of data transmission is determined by the level of the DIR input. The output enable pin ($\overline{OE}$) can be used to disable the device, so that the buses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

- High Speed: t_{PD} = 4.0 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 308 FETs or 77 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant
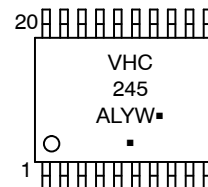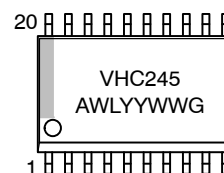
APPLICATION NOTES

- Do not force a signal on an I/O pin when it is an active output, damage may occur.
- All floating (high impedance) input or I/O pins must be fixed by means of pull up or pull down resistors or bus terminator ICs.
- A parasitic diode is formed between the bus and V_{CC} terminals. Therefore, the VHC245 cannot be used to interface 5 V to 3 V systems directly.

MARKING DIAGRAMS

SOIC−20
DW SUFFIX
CASE 751D

20
VHC245
AWLYYWWG
1

TSSOP−20
DT SUFFIX
CASE 948E

20
VHC
245
ALYW■
■
1

VHC245	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ■	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping[†]
MC74VHC245DWG	SOIC−20	38 Units/Rail
MC74VHC245DTG	TSSOP−20	75 Units/Rail
MC74VHC245DWR2G	SOIC−20	1000 Units/Reel
MC74VHC245DTR2G	TSSOP−20	2500 Units/T&R

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
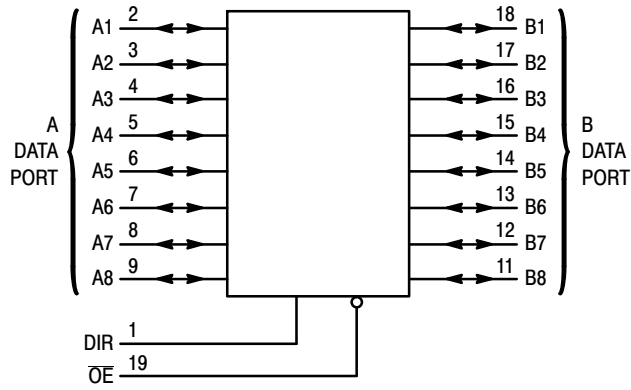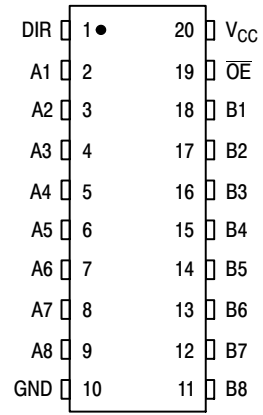
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Figure 1. LOGIC DIAGRAM

Figure 2. PIN ASSIGNMENT

FUNCTION TABLE

Control Inputs		Operation
$\overline{OE}$	DIR	
L	L	Data Transmitted from Bus B to Bus A
L	H	Data Transmitted from Bus A to Bus B
H	X	Buses Isolated (High−Impedance State)

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage	− 0.5 to + 7.0	V
V_{out}	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	− 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device
 may occur. Exposure to these conditions or conditions beyond those indicated may
 adversely affect device reliability. Functional operation under absolute−maximum−rated
 conditions is not implied.

†Derating ─ SOIC Packages: − 7 mW/°C from 65° to 125°C
                     TSSOP Package: − 6.1 mW/°C from 65° to 125°C

> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
>
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		− 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V V_{CC} =5.0V ±0.5V	0 0	100 20	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = − 40 to 85°C Min	T_A = − 40 to 85°C Max	Unit
V_{IH}	Minimum High−Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low−Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = − 50µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = − 4mA I_{OH} = − 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5 V or GND (DIR, $\overline{OE}$)	0 to 5.5			± 0.1		± 1.0	µA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	$T_A = 25°C$			$T_A = -40$ to $85°C$		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three−State Leakage Current	$V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

Symbol	Parameter	Test Conditions		$T_A = 25°C$			$T_A = -40$ to $85°C$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to B or B to A	$V_{CC} = 3.3 ± 0.3$V	$C_L = 15$pF $C_L = 50$pF		5.8 8.3	8.4 11.9	1.0 1.0	10.0 13.5	ns
		$V_{CC} = 5.0 ± 0.5$V	$C_L = 15$pF $C_L = 50$pF		4.0 5.5	5.5 7.5	1.0 1.0	6.5 8.5	
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OE}$ to A or B	$V_{CC} = 3.3 ± 0.3$V $R_L = 1$ kΩ	$C_L = 15$pF $C_L = 50$pF		8.5 11.0	13.2 16.7	1.0 1.0	15.5 19.0	ns
		$V_{CC} = 5.0 ± 0.5$V $R_L = 1$ kΩ	$C_L = 15$pF $C_L = 50$pF		5.8 7.3	8.5 10.6	1.0 1.0	10.0 12.0	
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OE}$ to A or B	$V_{CC} = 3.3 ± 0.3$V $R_L = 1$ kΩ	$C_L = 50$pF		11.5	15.8	1.0	18.0	ns
		$V_{CC} = 5.0 ± 0.5$V $R_L = 1$ kΩ	$C_L = 50$pF		7.0	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	$V_{CC} = 3.3 ± 0.3$V (Note 1)	$C_L = 50$pF			1.5		1.5	ns
		$V_{CC} = 5.0 ± 0.5$V (Note 1)	$C_L = 50$pF			1.0		1.0	ns
C_{in}	Maximum Input Capacitance DIR, $\overline{OE}$				4	10		10	pF
$C_{I/O}$	Maximum Three−State I/O Capacitance				8				pF

		Typical @ 25°C, $V_{CC} = 5.0$V	
C_{PD}	Power Dissipation Capacitance (Note 2)	21	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC} / 8$ (per bit). C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} • V_{CC}^2 • f_{in} + I_{CC} • V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ns, $C_L = 50$pF, $V_{CC} = 5.0$V)

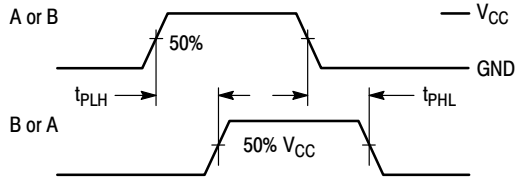| Symbol	Parameter	$T_A = 25°C$		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.9	1.2	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.9	−1.2	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

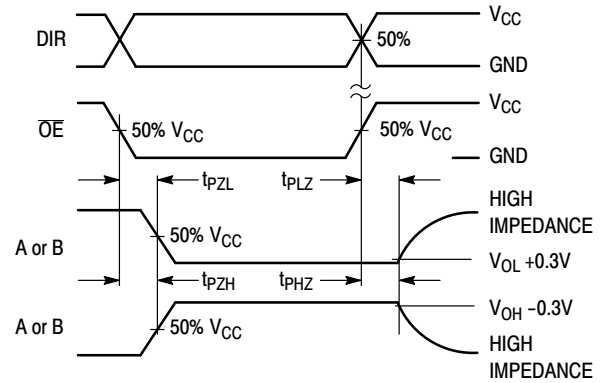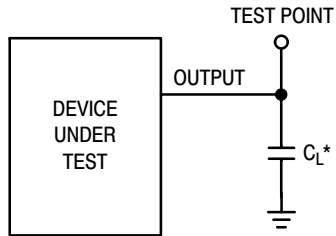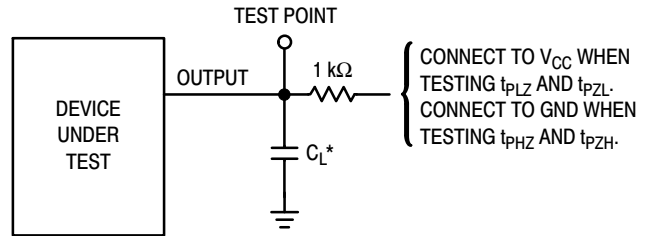## SWITCHING WAVEFORMS

Figure 3.

Figure 4.

TEST CIRCUITS

*Includes all probe and jig capacitance

Figure 5.

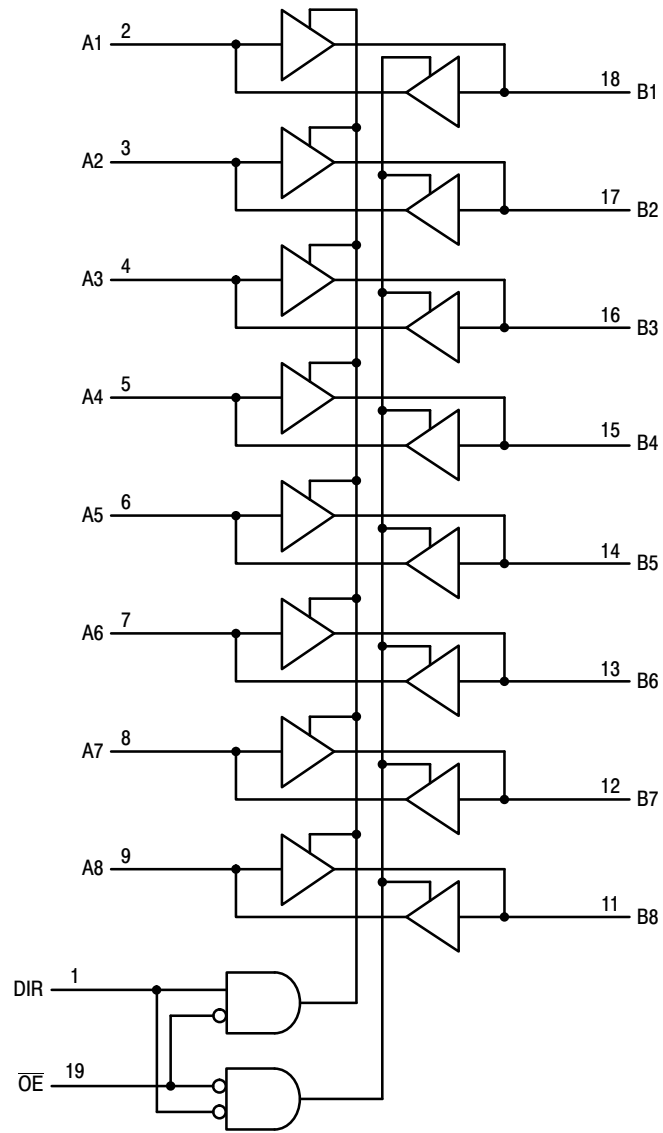*Includes all probe and jig capacitance

Figure 6.
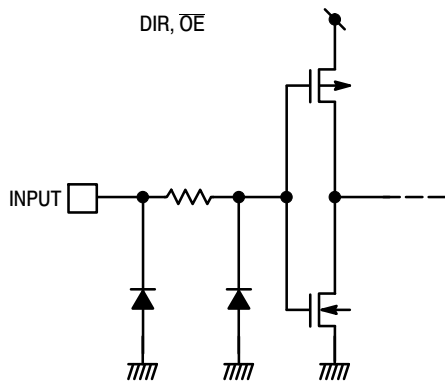
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Figure 7. EXPANDED LOGIC DIAGRAM
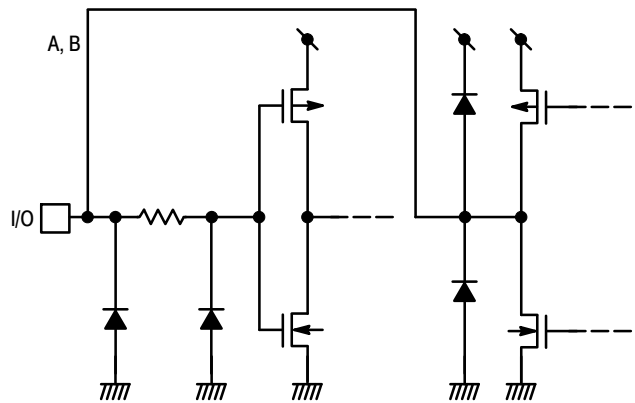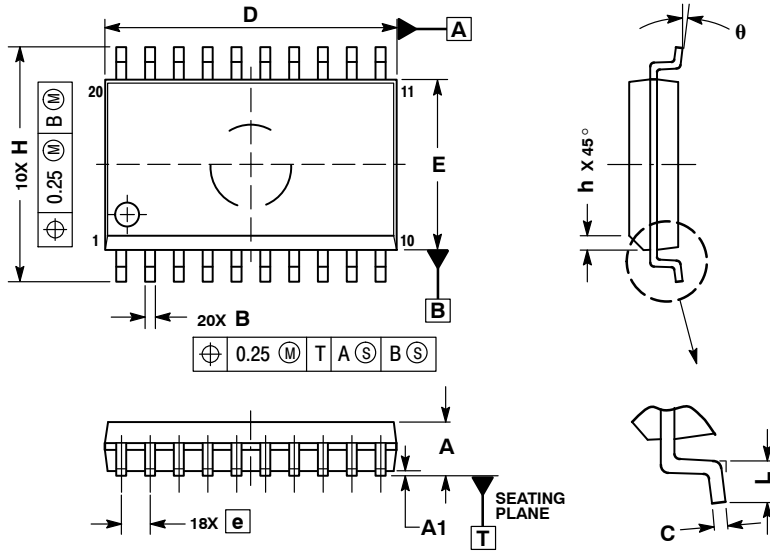

Figure 8. INPUT EQUIVALENT CIRCUIT

Figure 9. BUS TERMINAL EQUIVALENT CIRCUIT

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PACKAGE DIMENSIONS
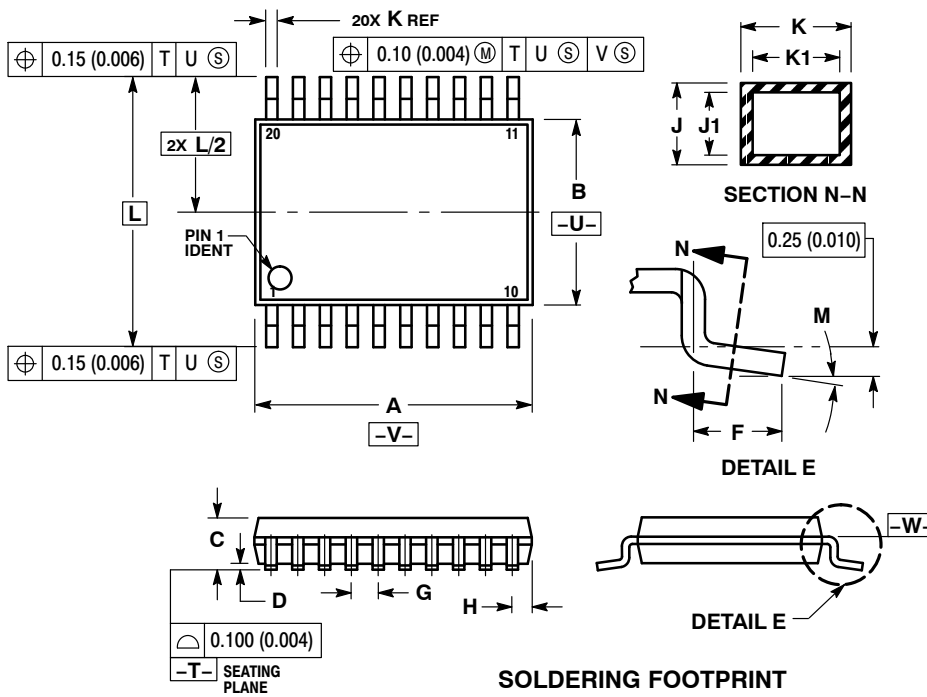
SOIC−20
CASE 751D−05
ISSUE G

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0 °	7 °

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PACKAGE DIMENSIONS

TSSOP−20
CASE 948E−02
ISSUE C

SECTION N−N

DETAIL E

0.25 (0.010)

SOLDERING FOOTPRINT

7.06

16X 0.36

16X 1.26

0.65 PITCH

DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

MC74VHC245/D