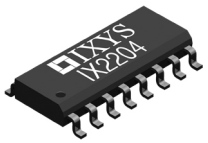
IXYS
INTEGRATED CIRCUITS DIVISION



IX2204
Dual Low Side IGBT Gate Driver

Features

- High Output Current: 2A Source/4A Sink
- Wide Operating Voltage Range: -10V to +26V
- Negative Gate Drive Capability
- Desaturation Detection Circuit
- Separate Source and Sink Outputs
- Programmable Blanking and Output Tristate
- TTL Compatible Inputs
- -40°C to +125°C Extended Operating Temperature Range
- Under-Voltage Lockout Circuitry
- Fault Status Output

Applications

- Efficient IGBT Switching
- Motor Controls
- Switch Mode Power Supplies

Description

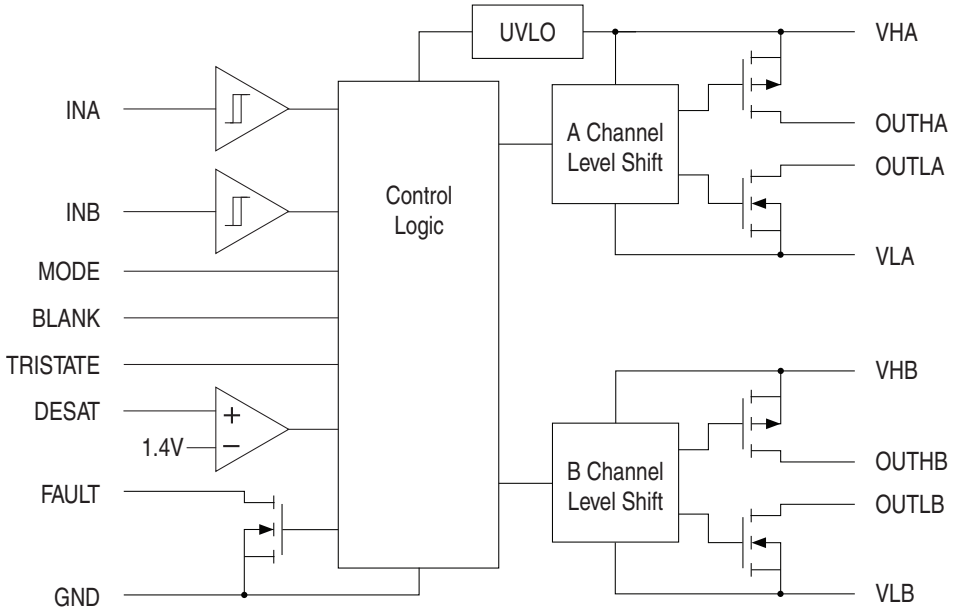
The IX2204 is a dual high current gate driver specifically designed to drive the gates of high current IGBTs. The IX2204 provides two high current outputs capable of sourcing 2A and sinking 4A. The outputs can be paralleled for IGBT gates that require higher drive current. The outputs have a wide operating voltage range, and are able to provide a negative gate drive voltage to ensure the turn-off of high power IGBTs. A desaturation detection circuit protects the power IGBT during a short circuit. The IX2204 has a programmable two-level turn-off feature that protects the device against excessive voltages when the IGBT is being turned off due to an over-current situation.

The IX2204 has under voltage lockout circuitry and a fault status output, and is available in a 16-lead thermally enhanced SOIC package.

Ordering Information

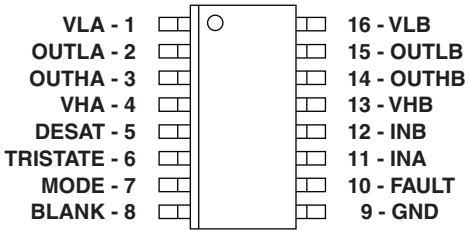
Part	Description
IX2204NE	16-Pin SOIC in Tubes (50/Tube)
IX2204NETR	16-Pin SOIC in Tape & Reel (2000/Reel)

IX2204 Functional Block Diagram



1 Specifications

1.1 Package Pinout: 16-Pin SOIC Package



1.2 Pin Description: 16-Pin SOIC Package

Pin#	Name	Description
1	VLA	Channel A negative supply
2	OUTLA	Channel A sinking output
3	OUTHA	Channel A sourcing output
4	VHA	Channel A positive supply & logic supply
5	DESAT	Desaturation comparator input
6	TRISTATE	Channel A tristate timing
7	MODE	Mode control
8	BLANK	Channel A start-up blanking time
9	GND	Signal ground
10	FAULT	Fault status output
11	INA	Channel A logic input
12	INB	Channel B logic input
13	VHB	Channel B positive Supply
14	OUTHB	Channel B sourcing output
15	OUTLB	Channel B sinking output
16	VLB	Channel B negative supply

1.3 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
VH Supply Voltage [1]	VHA, VHB	-	26	V
VL Supply Voltage	VLA, VLB	-10	-	V
Supply Voltage All Other Pins	-	GND-0.3	VHA+0.3	V
Output Sourcing Current	I_{OUTH}	-	-2	A
Output Sinking Current	I_{OUTL}	-	4	A
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-65	+150	°C

Note 1: VHx-VLx maximum is 26V.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
VH Supply Voltage	VHA, VHB	-	25	V
VL Supply Voltage	VLA, VLB	-10	GND	V
Operating Temperature Range	T_A	-40	+125	°C

1.5 DC Electrical Characteristics

13V ≤ VHA ≤ 25V; 13V≤VHB≤25V; -40°C≤T_A≤125°C.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Power Supply Current	VHA=18V	I_{VHA}	-	-	3.5	mA
Under-Voltage Lockout Output Enable Threshold	VHA Rising	UVLO+	10	-	13	V
Under-Voltage Lockout Output Hysteresis	-	$UVLO_{HYS}$	-	1	-	V
INA / INB Logic Low Threshold	-	V_{IL}	0.8	-	-	V
INA / INB Logic High Threshold	-	V_{IH}	-	-	2	V
INA / INB / MODE Input Current	-	I_{IN}	-	-	1	µA
DESAT Threshold	-	V_{DESAT}	1.26	1.4	1.54	V
TRISTATE / BLANK Source Current	-	I_{SRC}	-100	-160	-210	µA
FAULT Output						
FAULT Low Voltage	I_{FAULT}=8mA	V_{FAULT}	-	-	0.8	V
Outputs						
Low Output Voltage	No Load	V_{OUTL}	-	-	VL+0.025	V
High Output Voltage	No Load	V_{OUTH}	VH-0.025	-	-	V
Output Resistance	VH=18V, I_{OUTH}= -100mA	R_{OUTH}	-	2.4	5	Ω
	VH=18V, I_{OUTL}= 100mA	R_{OUTL}	-	1.2	2	Ω

1.6 AC Electrical Characteristics

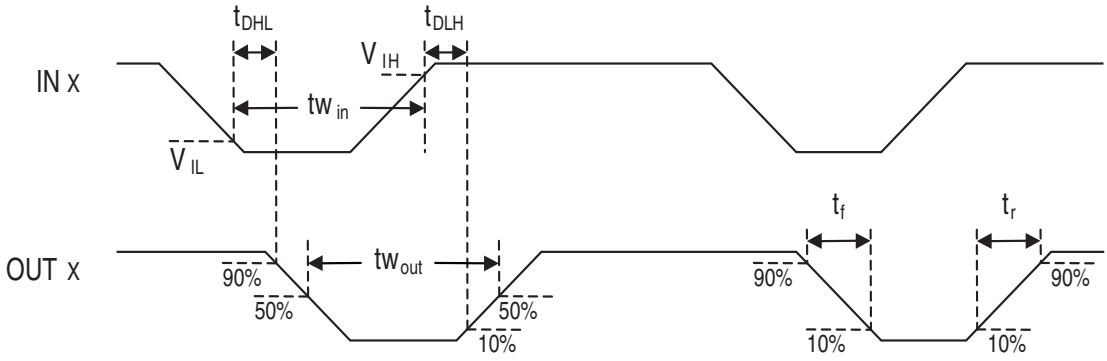
13V ≤ VHA ≤ 25V; -40°C≤T_A≤125°C

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
OUT Rise Time	VH=18V, C_{LOAD}=1nF	t_r	-	-	40	ns
OUT Fall Time		t_f	-	8	20	
Delay, IN to OUT Rising		TDLH	-	70	100	
Delay, IN to OUT Falling		TDHL	-	70	100	
IN to OUT Pulse Distortion	(tw_{in} - tw_{out}), C_{LOAD}=0	Δtw	-	7	25	ns
	(tw_{in} - tw_{out}), C_{LOAD}=1nF		-	7	25	
DESAT Blank Time	C_{BLANK}=0	t_{BLANK}	-	-	100	ns
	C_{BLANK}=100pF		-	875	-	
Delay Time, DESAT to Output Tristate	R_L=100Ω to GND	t_{DELAY1}	-	50	100	ns
Duration of Tristate OUT	$C_{TRISTATE}$=0	$t_{TRISTATE}$	-	-	100	ns
	$C_{TRISTATE}$=100pF		-	1000	-	
Delay Time, TRISTATE high to OUT Low	VH=18V, C_{LOAD}=1nF	t_{DELAY2}	-	-	100	ns

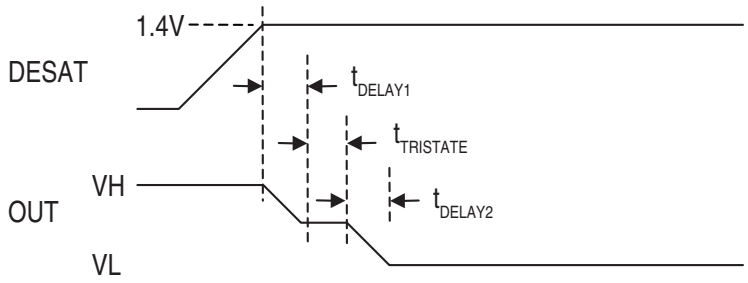
1.7 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Resistance, Junction to Ambient	θ_{JA}	75.4	°C/W

1.8 AC Input/Output Timing Diagram (MODE=0V)

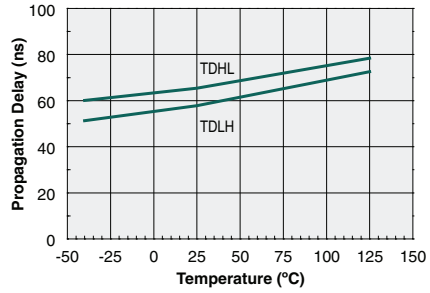


1.9 AC Fault Timing Diagram

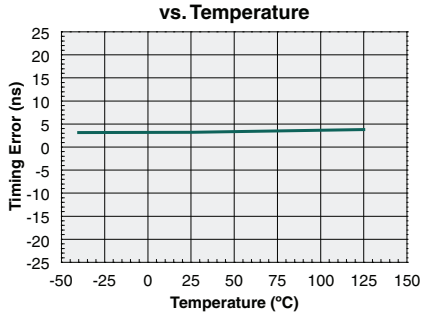


2 Performance Characteristics

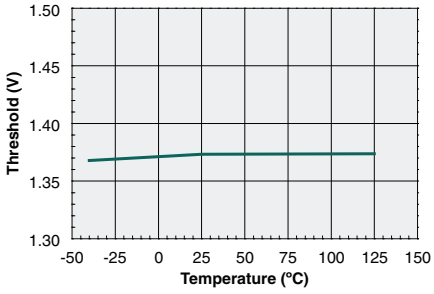
Propagation Delay vs. Temperature



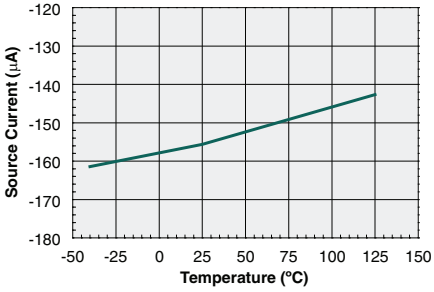
Pulse Width Distortion vs. Temperature



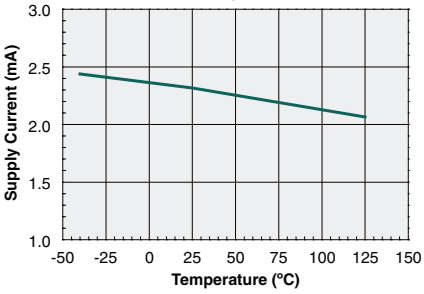
V_{DESAT} Threshold vs. Temperature



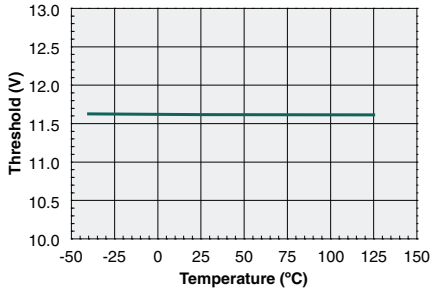
TRISTATE and BLANK Source Current vs. Temperature



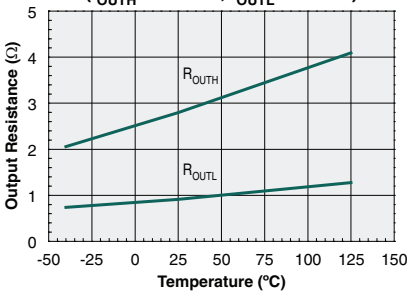
Power Supply Current vs. Temperature



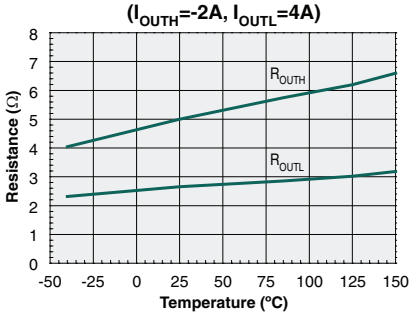
UVLO+ Threshold vs. Temperature



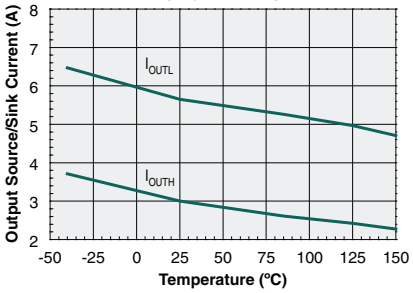
Output Resistance vs. Temperature (I_{OUTH}=-100mA, I_{OUTL}=100mA)



Output Resistance vs. Temperature (I_{OUTH}=-2A, I_{OUTL}=4A)



Peak Output Current vs. Temperature (10µs Pulse)



3 Functional Description

3.1 Input

The INA and INB inputs are TTL compatible and must be referenced to GND.

3.2 Mode

The MODE input determines how the desaturation protection and Under-Voltage Lock Out (UVLO) protection circuitry controls the OUTHA, OUTLA, OUTHB and OUTLB outputs. For parallel-mode IGBT drive, MODE should be connected to GND (see 4.1). For driving IGBTs that require higher gate drive current than the IX2204 can provide, the IX2204 can be used to control external drive transistors. In this stacked configuration, the external drive transistors constitute an inverting stage, and MODE should be connected to VHA for proper desaturation protection and UVLO operation (see 4.3).

3.3 Desaturation Protection

The desaturation protection circuit ensures the protection of an external IGBT in the event of an over-current situation. When the voltage at DESAT exceeds 1.4V (typically) and MODE is connected to GND, OUTLA and OUTLB are driven low in a two-step process. First OUTLA, OUTHA, OUTLB and OUTHB are all turned off (high impedance). Then after a programmable time ($t_{TRISTATE}$), both OUTLA and OUTLB are turned on (driven low), which quickly turns off the IGBT. This two-step action avoids both dangerous over-voltages across the IGBT and reverse-bias SOA problems, especially during a short circuit turn-off. The time that all the outputs are in tristate is set by an internal current source and an external capacitor (CTRISTATE) that is connected to the TRISTATE pin. The tristate time is approximately:

$$t_{TRISTATE} = 8750 \bullet C_{TRISTATE}$$

The desaturation circuit is disabled for a fixed blanking time to avoid detecting a false desaturation event during IGBT turn-on, thus allowing enough time for IGBT saturation. This blanking time is set by an internal current source and an external capacitor, C_{BLK}. The blanking time is approximately:

$$t_{BLK} = 8750 \bullet C_{BLK}$$

This blanking time starts when INA transitions from low to high.

The desaturation two-step turn off is slightly different when MODE is connected to VHA for stack-mode IGBT drive. When the DESAT voltage exceeds 1.4V, OUTHA and OUTLB are turned on, tristating the IGBT. After the $t_{TRISTATE}$ time, OUTHA and OUTLB are turned off, and OUTHB is turned on, which in conjunction with the external drive transistor quickly turns off the IGBT. When MODE is connected to VHA, the blanking time starts when INA transitions from high to low.

The desaturation protection circuit cannot be used when the IX2204 is used to drive two separate IGBTs (direct IGBT drive, see 4.2). When driving two separate IGBTs, the DESAT, TRISTATE, MODE, and BLANK pins should all be connected to GND.

3.4 Under-Voltage Protection

The Under Voltage Lock Out (UVLO) circuit protects the IGBT from insufficient gate voltage. The UVLO circuit monitors the VHA supply voltage. If MODE is connected to GND and VHA is below the UVLO+ threshold, OUTHA and OUTHB are both turned-off (high impedance), and both OUTLA and OUTLB are both turned on (pulled low). If VHA is below the UVLO+ threshold and MODE is connected to VHA, OUTHA and OUTHB are both are turned on, and OUTLA and OUTLB are both turned off.

Table 2: Output States with VHA < UVLO+

Mode	OUTHA	OUTLA	OUTHB	OUTLB
GND	Z	0	Z	0
VHA	1	Z	1	Z

3.5 Fault Output

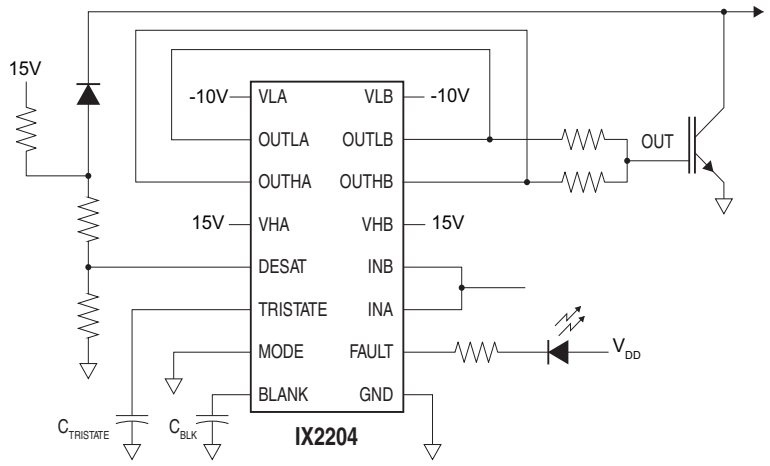
The FAULT output is pulled low during a desaturation event, or when VHA is below UVLO+.

3.6 Outputs

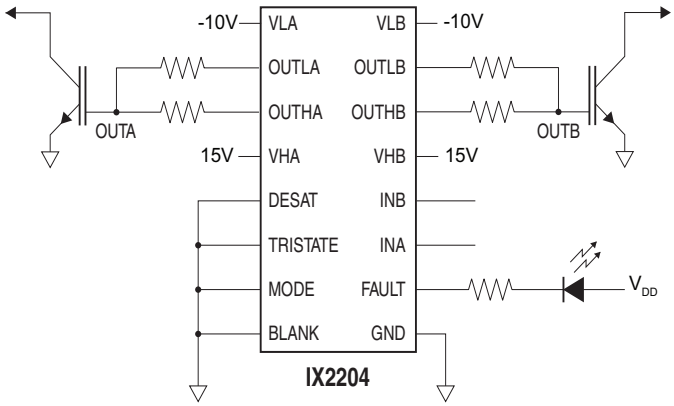
The output stages are able to source 2A, and sink 4A. Separated sink and source outputs allow independent gate charge and discharge control. For higher gate drive applications, the source and sink outputs can be paralleled to source 4A, and sink 8A.

4 Application Drawings

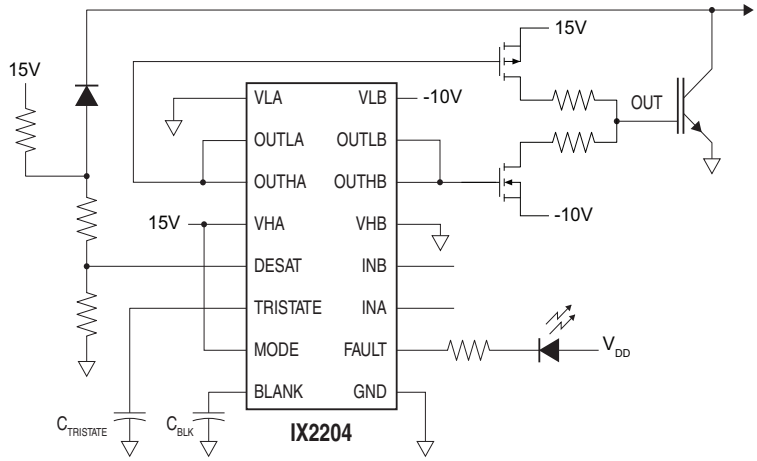
4.1 Parallel-Mode IGBT Drive with Desaturation Detection



4.2 Direct IGBT Drive



4.3 Stack-Mode IGBT Drive with Desaturation Detection



5 Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
IX2204NE	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

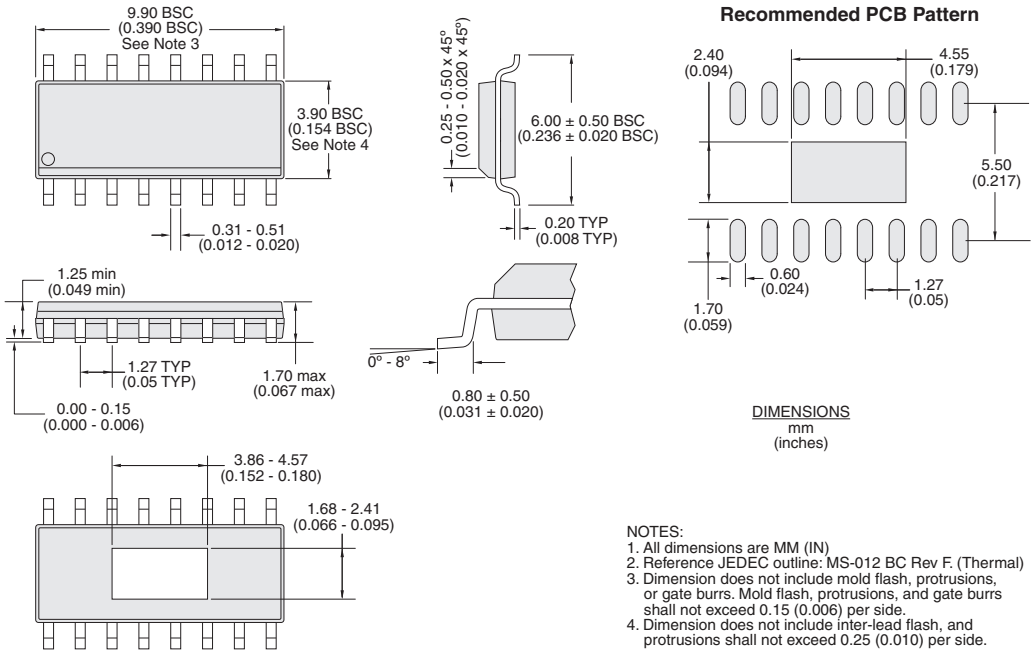
Device	Maximum Temperature x Time	Maximum Reflow Cycles
IX2204NE	260°C for 30 seconds	3

5.4 Board Wash

IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

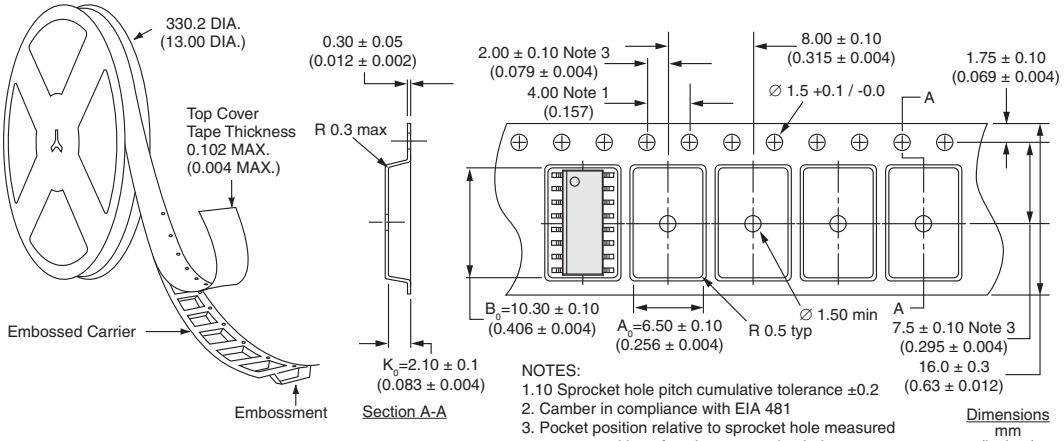
5.5 Mechanical Dimensions

5.5.1 IX2204NE 16-Pin Narrow SOIC Package



NOTES:
1. All dimensions are MM (IN)
2. Reference JEDEC outline: MS-012 BC Rev F. (Thermal)
3. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 (0.006) per side.
4. Dimension does not include inter-lead flash, and protrusions shall not exceed 0.25 (0.010) per side.

5.5.2 IX2204NETR Tape & Reel Packaging for 16-Pin Narrow SOIC Package (TBD)



NOTES:
1.10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

For additional information please visit our website at: www.ixysic.com

Specification: DS-IX2204-R03

11/11/2014